18-622 Final Project

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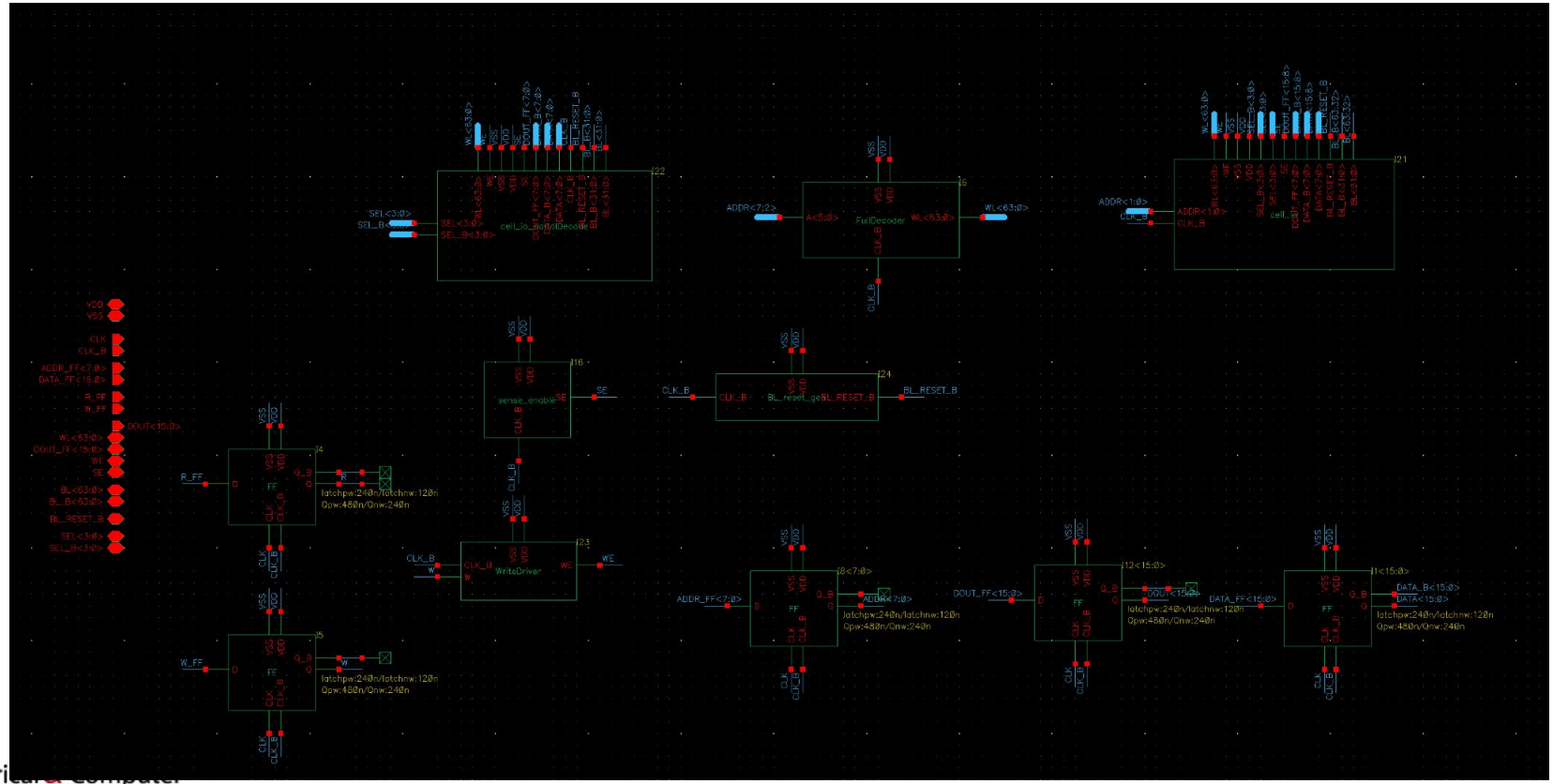
Schematics

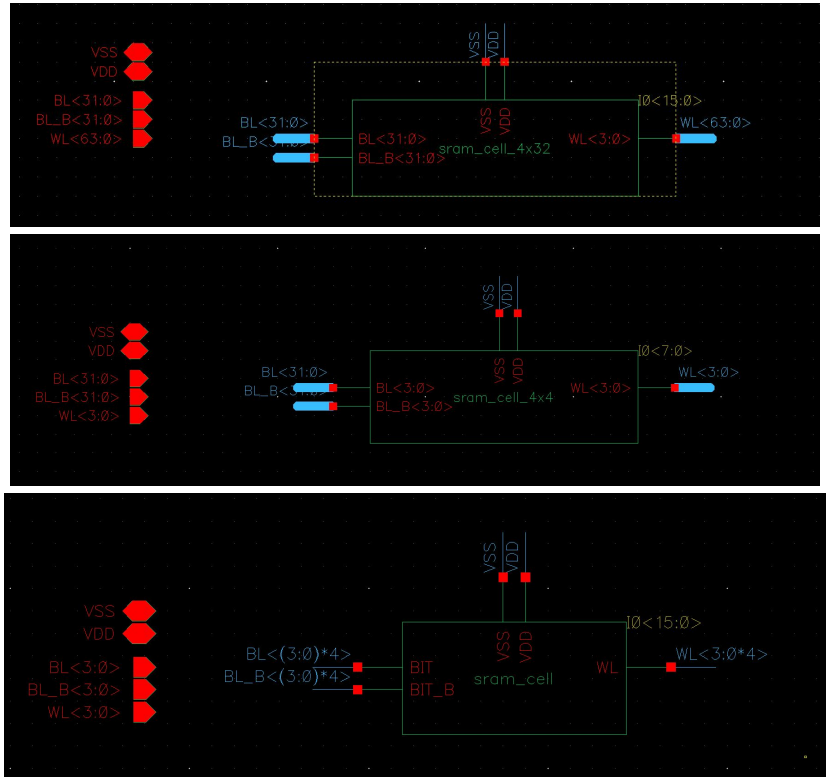
Schematics Guideline

- Put screenshots for
  - Full block schematic
  - Array
  - Cell
  - Address Decoder
  - Write Driver, Bitline Reset
  - Column mux
  - Sense Amp
- Can use multiple slides for the screenshots
- Show screenshot of estimated wire model schematic
- Please share features in your schematic that you think are special or unique

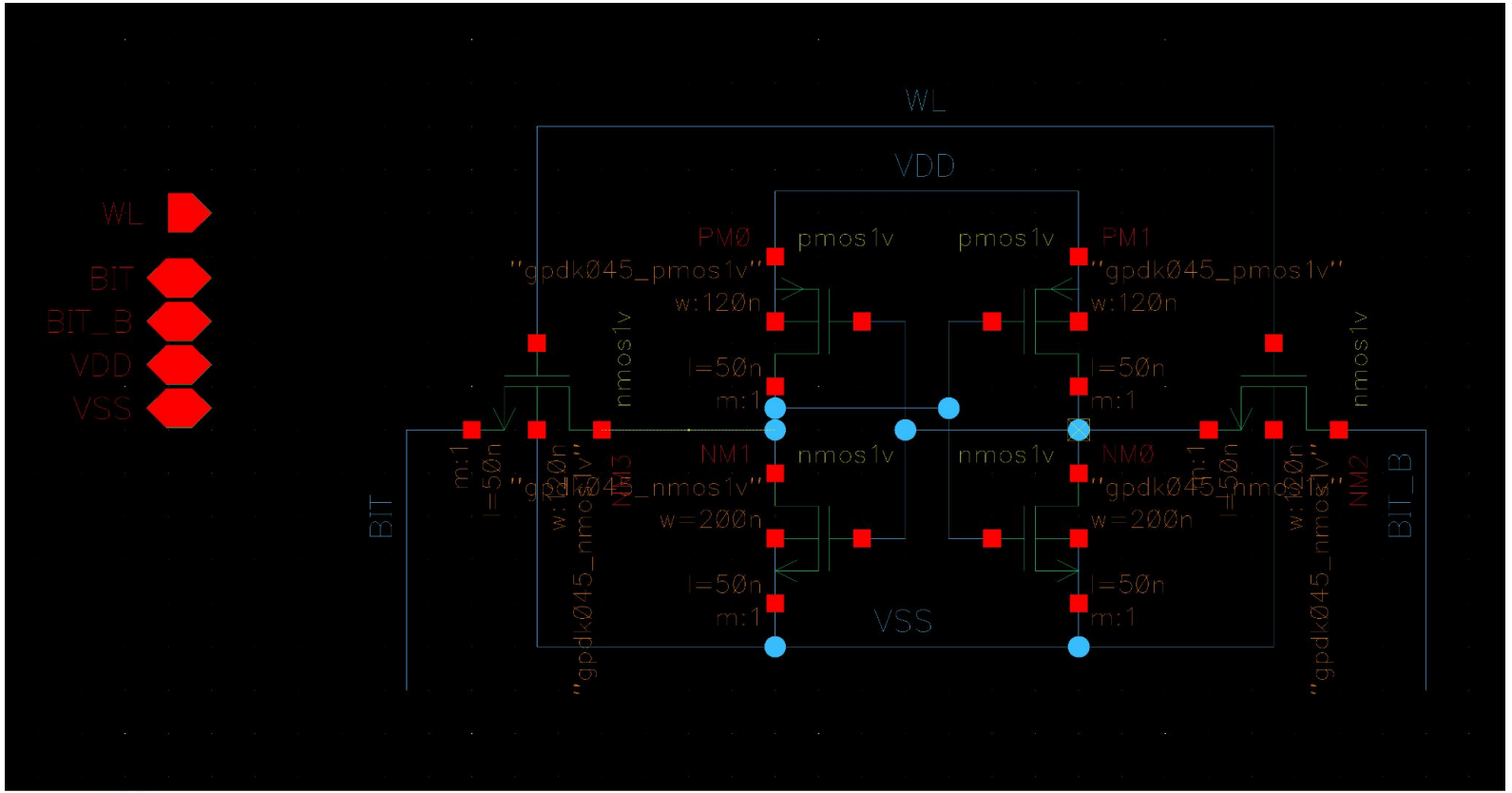
Full block schematic



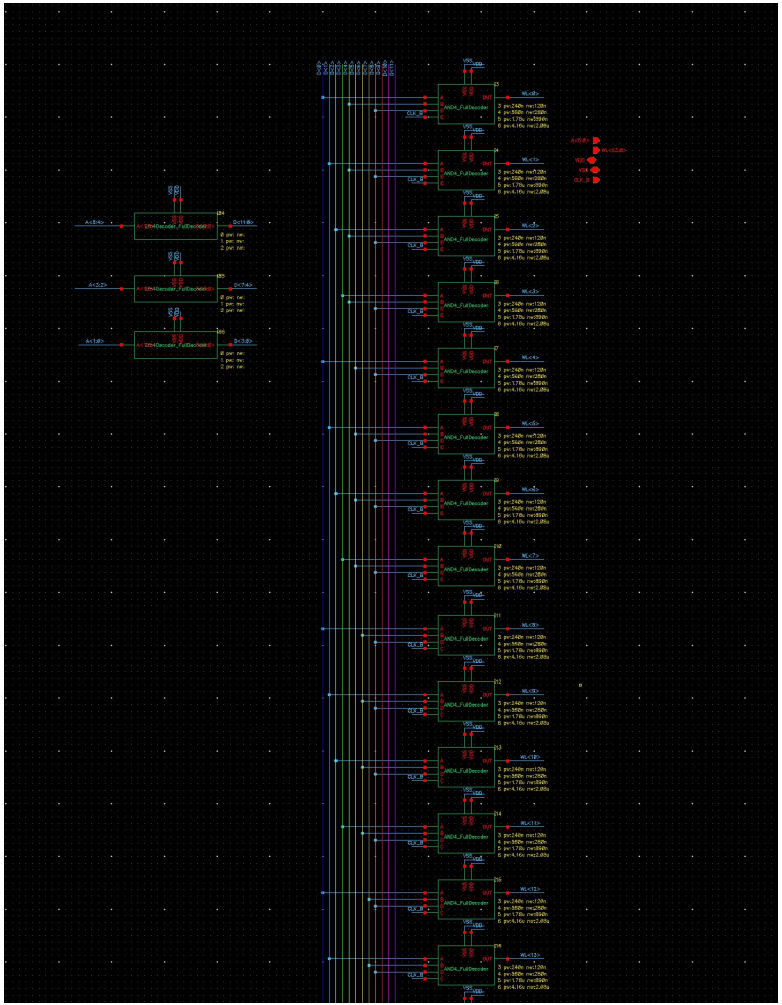
Array


VSS
VDD
BL<31:0>
BL_B<31:0>
WL<63:0>
sram_cell_4x32
I0<15:0>
WL<3:0>
I0<7:0>
BL<3:0>
BL_B<3:0>
sram_cell_4x4
BL<(3:0)*4>
BL_B<(3:0)*4>
BIT
BIT_B
sram_cell
WL
WL<3:0*4>

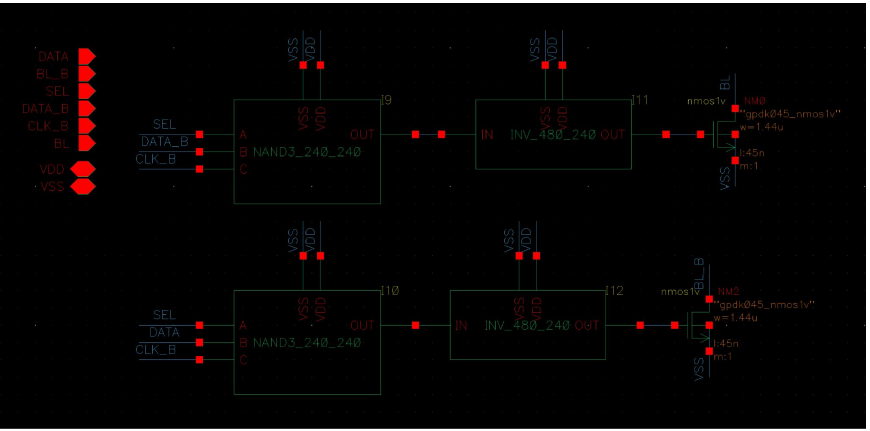
Cell

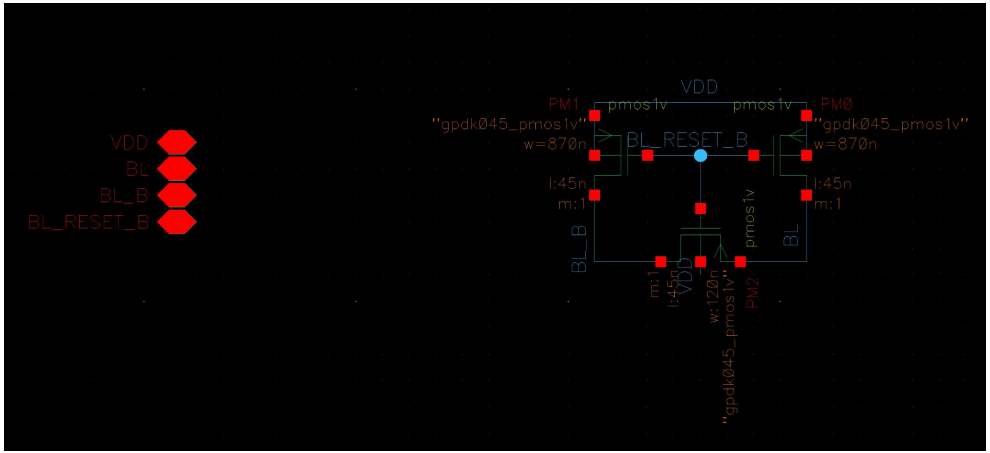

WL
BIT
BIT_B
VDD
VSS
WL
VDD
PM0
pmos1v
pmos1v
PM1
"gpdk045_pmos1v"
w:120n
l=50n
m:1
nmos1v
NM1
nmos1v
nmos1v
NM0
"gpdk045_nmos1v"
w=200n
VSS
BIT
BIT_B
NM3
NM2

Address Decoder

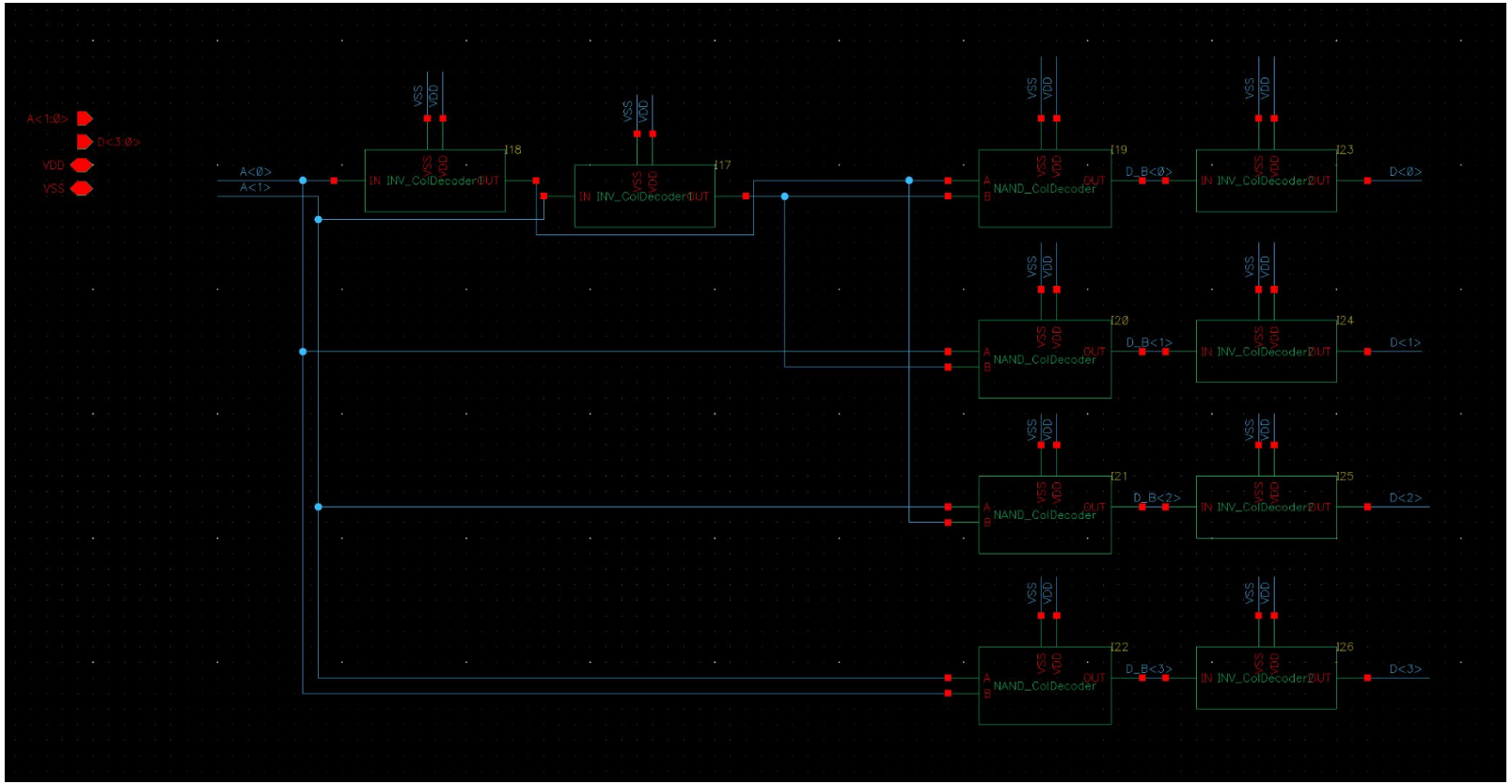


Write Driver, Bitline Reset

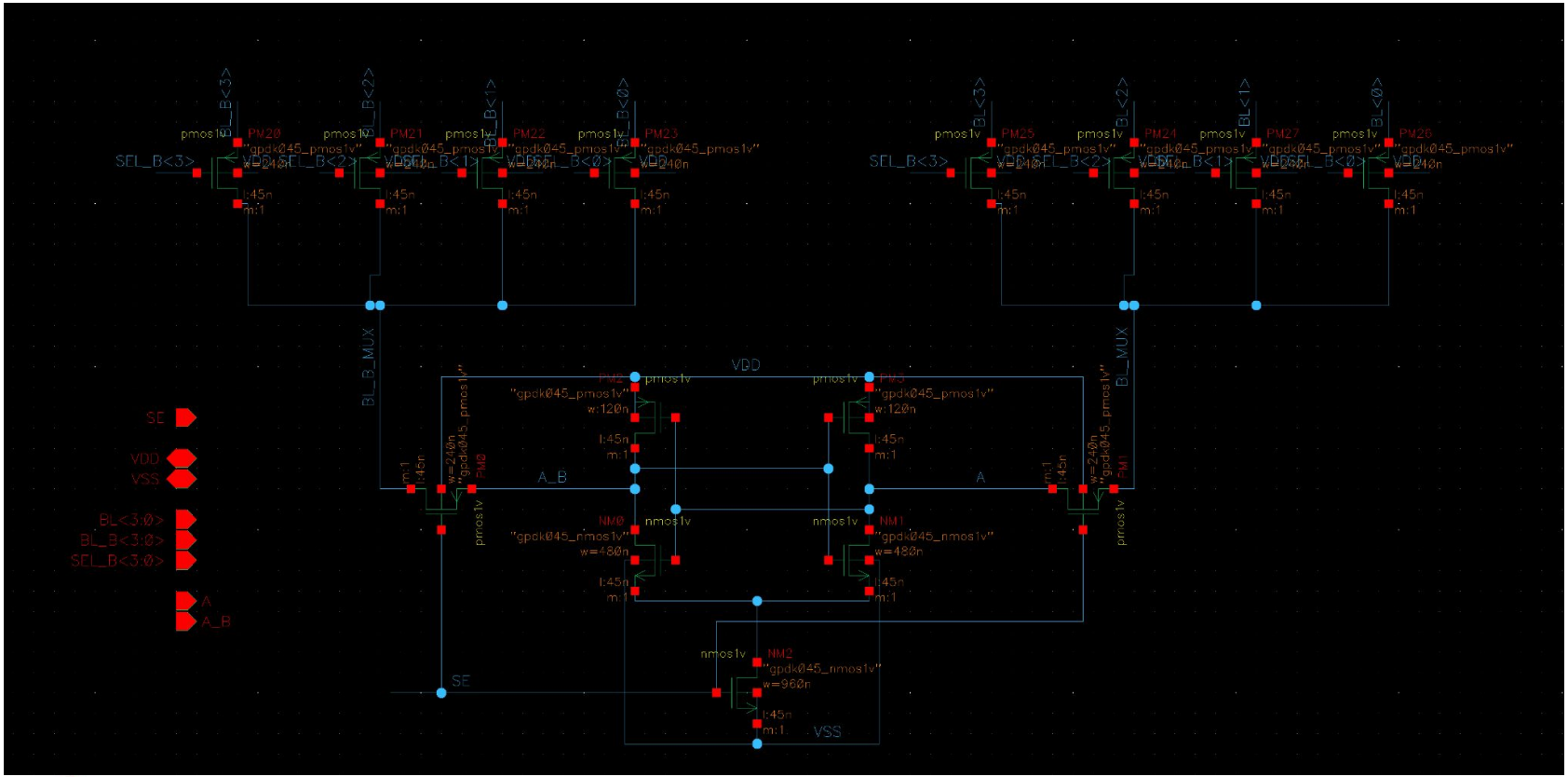




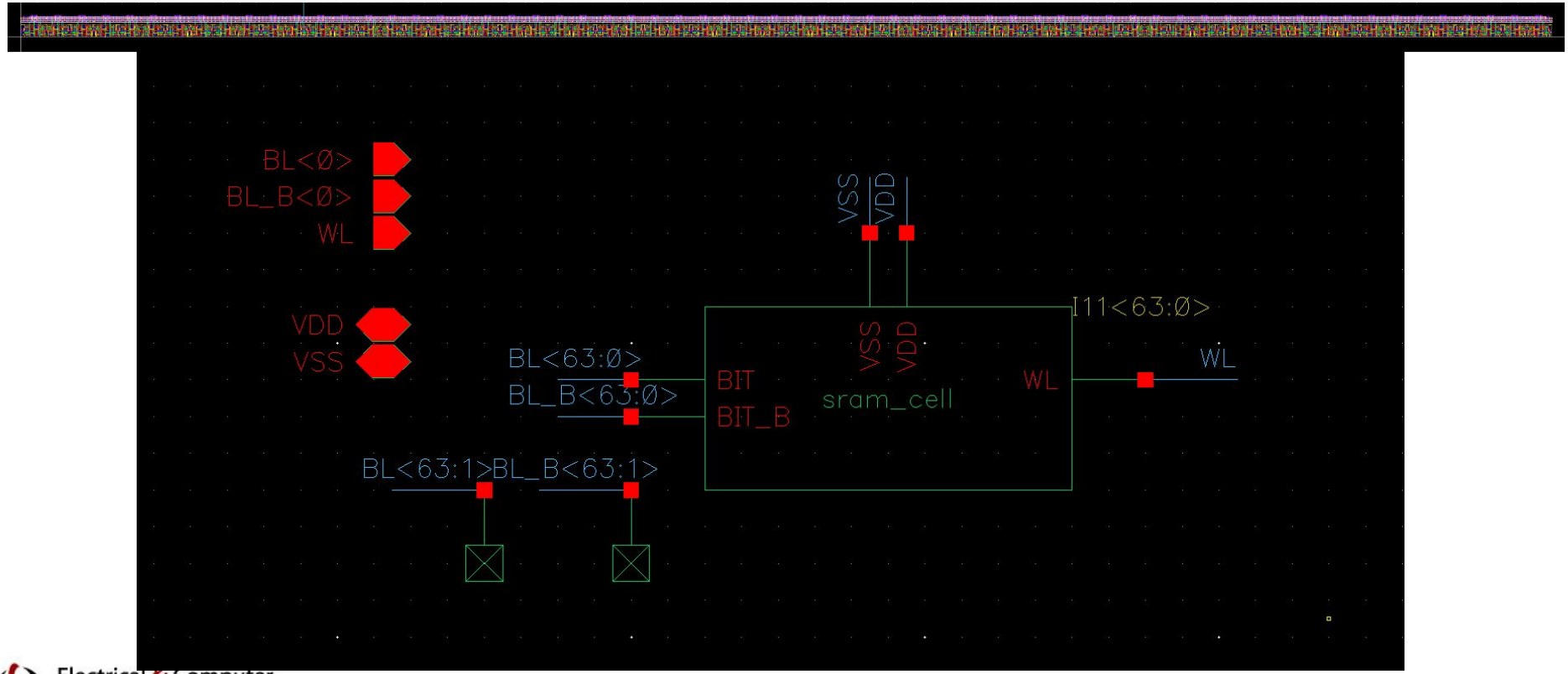
Column Mux


A<1:0>
D<3:0>
VDD
VSS
A<0>
A<1>
I18
I17
I19
I20
I21
I22
I23
I24
I25
I26
IN INV_ColDecoder1
OUT
NAND_ColDecoder
IN INV_ColDecoder2
D_B<0>
D_B<1>
D_B<2>
D_B<3>
D<0>
D<1>
D<2>
D<3>

Sense Amp


BL_B_MUX
BL_MUX
VDD
SE
VSS
BL<3:0>
BL_B<3:0>
SEL_B<3:0>
A
A_B
PM0
PM1
PM2
PM3
NM0
NM1
NM2
A_B
A
SE
VSS

Wire Model


BL<0>
BL_B<0>
WL
VDD
VSS
BL<63:0>
BL_B<63:0>
BL<63:1>
BL_B<63:1>
VSS
VDD
BIT
BIT_B
sram_cell
WL
I11<63:0>
WL

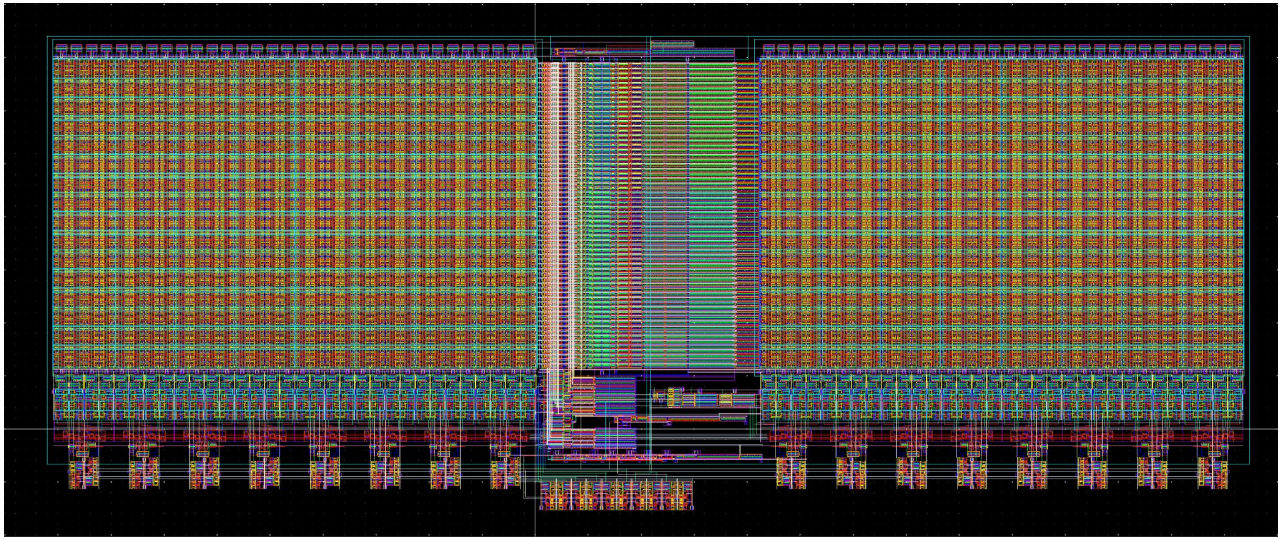
Layout

Layout Guidelines

- Screenshot of full block layout (if you have completed full block layout, otherwise show individual block layouts)
- Show rectilinear sizes for your full block and do area calculation
- Screenshot of all other important blocks that you think is necessary
- Screenshots of DRC and LVS passing

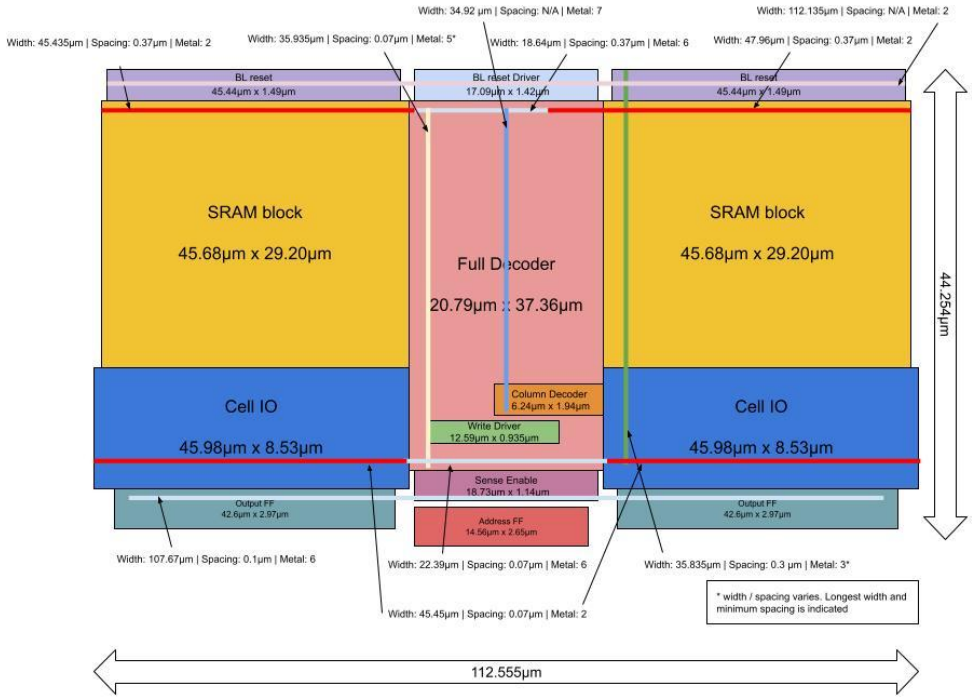
- Please share features in your layout that you think are special or unique

Full block (entire SRAM)



- Area: 4979.995975 um2 = 112.555 um * 44.245 um

Full block (entire SRAM)



Full block (entire SRAM)

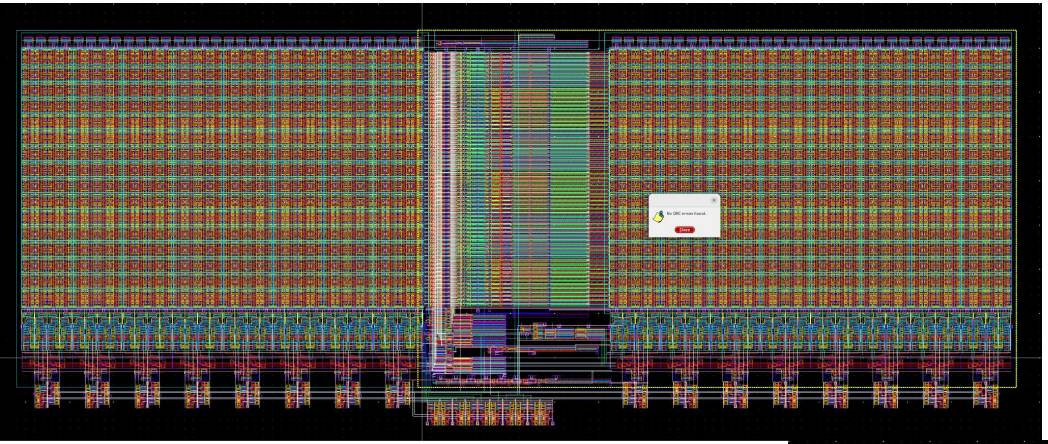
Total SRAM Cell Area: (45.68µm SRAM block width • 29.195µm SRAM block height) • 2 SRAM blocks = 2667.2552µm^2

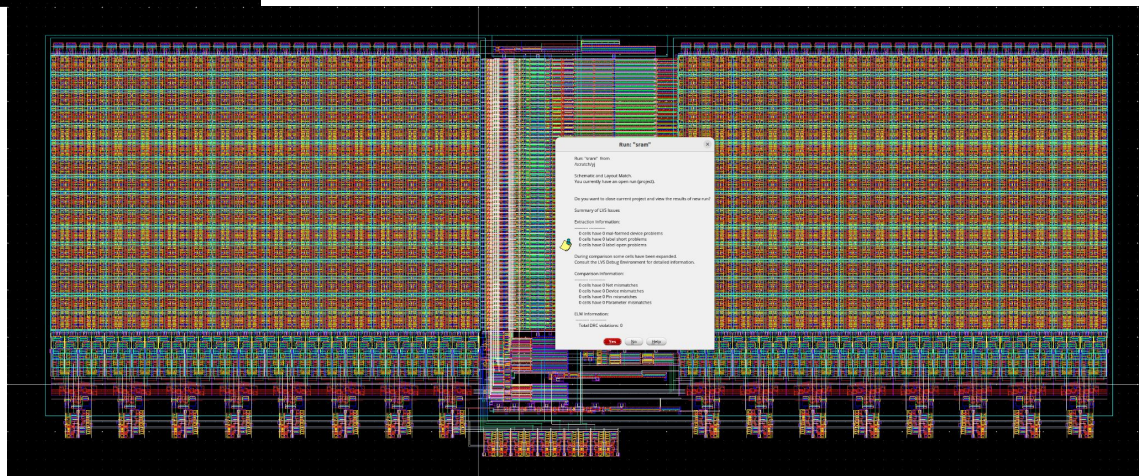
Total Area: (112.555µm full width • 44.245µm full height) = 4979.995975µm^2

Area efficiency: (Total SRAM Cell Area / Total Area) / 100 = (2667.2552µm^2 / 4979.995975µm^2) / 100 = 53.559%

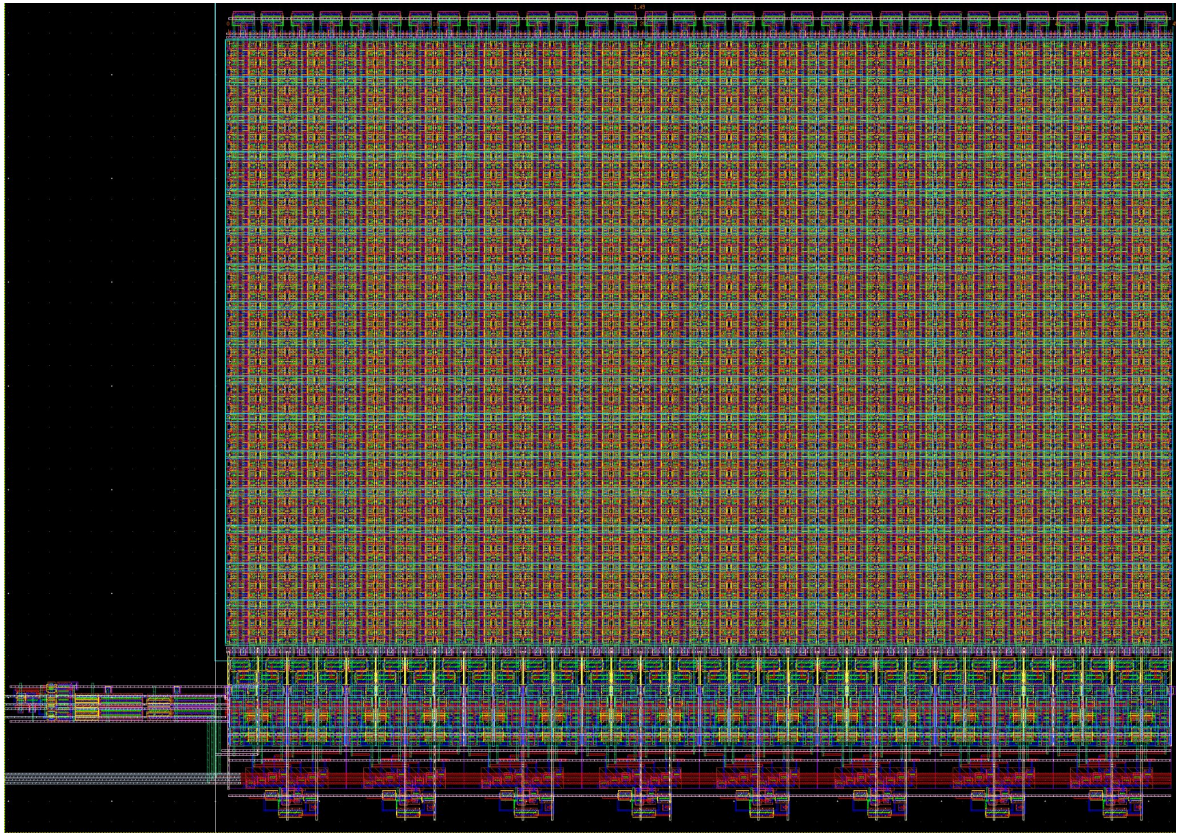
Lambda squared: (Total Area / λ^2) = (4979.995975µm^2 / 0.0225µm^2) ≈ 9.8M λ^2

Full block DRC and LVS results

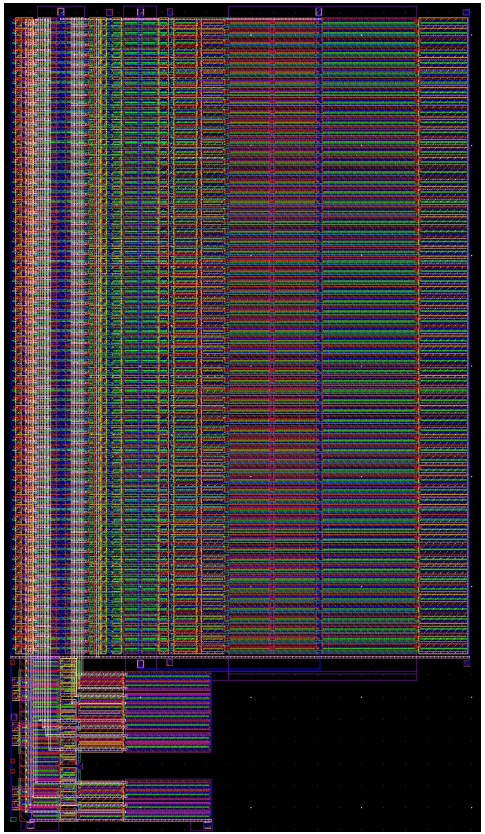




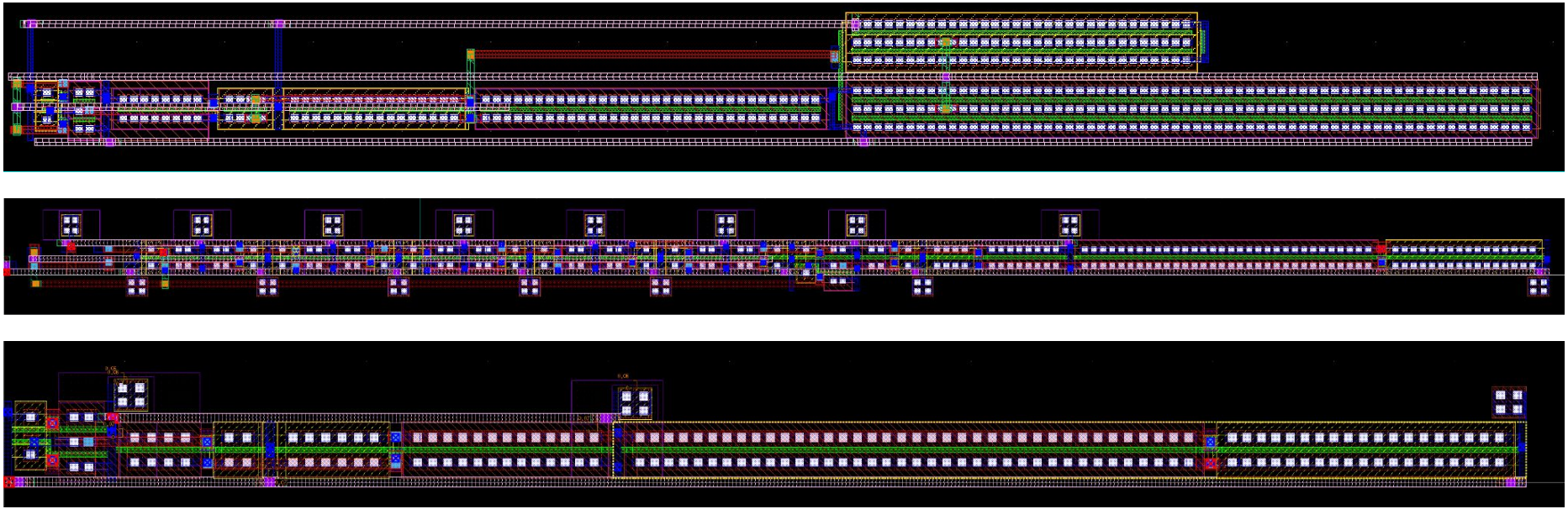
Cell IO, Column Decoder, and SRAM Block



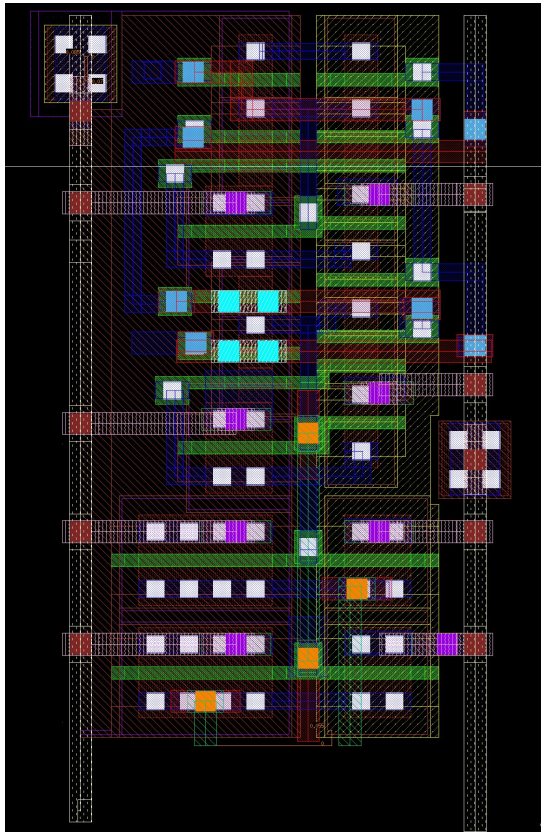
Row Decoder



Bitline reset, Write Driver, Sense Enable



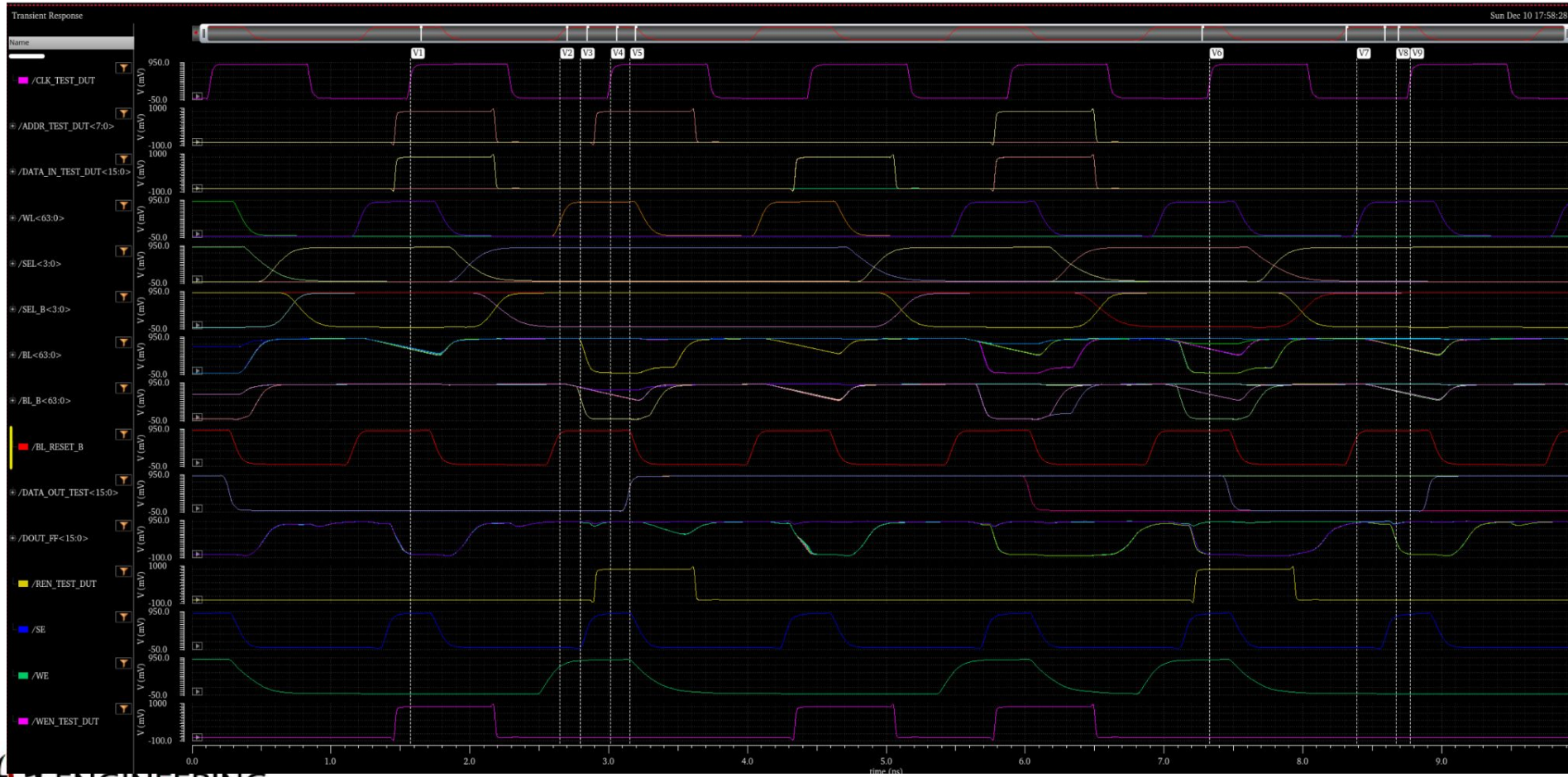
Flip Flop



Simulation

Simulation Results

- Results (Post layout sims if layout is complete)
  - If layout not complete, screenshots of full schematic sim or full sim with blocks that have complete layout
  - Must include important signals: WLs and BLs, controls (enough to comprehend R/W operation from just pictures)
  - Show delay markers in the simulation pictures for R/W ops
  - R/W ops must show critical path delay for each (you must determine/justify the test patterns to exercise the critical paths based on your design).


Transient Response
Sun Dec 10 17:58:28
Name
/CLK_TEST_DUT
/ADDR_TEST_DUT<7:0>
/DATA_IN_TEST_DUT<15:0>
/WL<63:0>
/SEL<3:0>
/SEL_B<3:0>
/BL<63:0>
/BL_B<63:0>
/BL_RESET_B
/DATA_OUT_TEST<15:0>
/DOUT_FF<15:0>
/REN_TEST_DUT
/SE
/WE
/WEN_TEST_DUT
V1
V2
V3
V4
V5
V6
V7
V8
V9
V (mV)
time (ns)

Live Demo (what we will be checking live)

- DRC run
- LVS run
- A ready ADE L sim window with all necessary signals
- Any other layout/schematic that we find necessary to check