Design and Tapeout of Image Sensor Pixel Array

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Abstract - This project focuses on the design and tapeout of a mixed-signal integrated circuit that can be used for image sensory in an IOT system. The chip is designed in TSMC's 65 nm technology with a die area of 1mm x 1mm. The primary goal of the project is to introduce the tapeout flow from start to finish as well as provide opportunities for mixed-signal design. The final chip has been simulated to ensure proper operation and reasonable performance; pass DRC and LVS to ensure a successful tapeout.

I. System Overview

The architecture of the system consists of an input Serial-In Parallel-Out (SIPO) scan chain for reading in digital 4-bit inputs for each pixel, a 5x3 image sensing pixel array, an output Parallel-In Serial-Out (PISO) scan chain for reading out 12-bit outputs from each pixel, and a global bias network for providing bias for analog blocks by scaling down an external current input. The details of the design specifications will be discussed in this paper later.

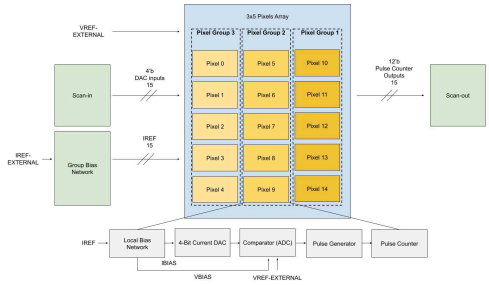


FIGURE I
SYSTEM BLOCKS DIAGRAM

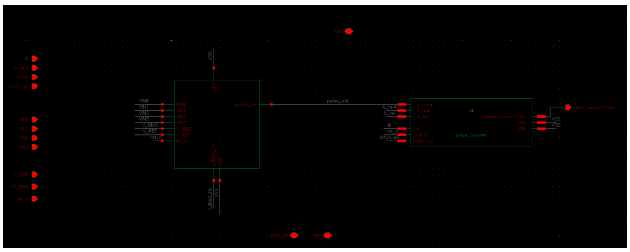
II. Design Process and Specifications

A. Schematics

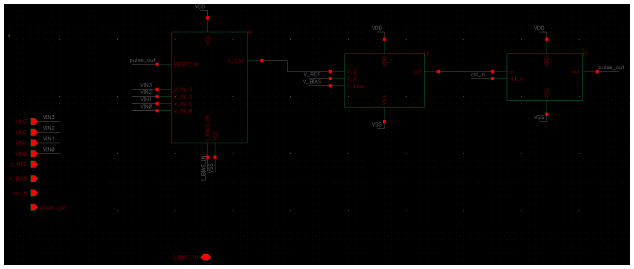
Each pixel's subblocks and specifications are as follows:

- A local bias generation circuit converts reference current from the group bias network to the bias current and voltage for DAC and comparator in each pixel
- A binary-weighted 4-bit current DAC feeding into a capacitor (this simulates the photosensitive part of the pixel) with a target ramp rate of 0.6 V/1µs
- A comparator is used as an ADC to signal a pulse generator to create a pulse with a target response time of 67ns
- A 12-bit counter is then used to count the number of pulses in a given clock cycle
- The counter output is sent to a scan chain to be read off the chip

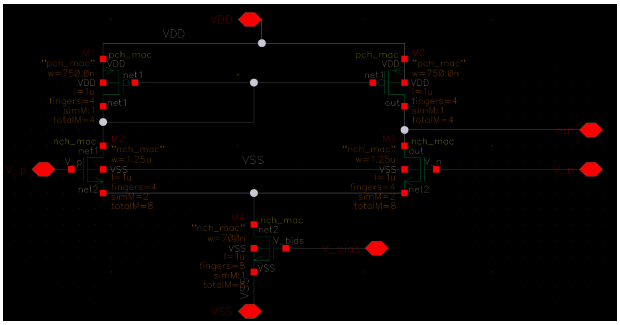
3 individual pixel designs were created by each of the group members. They were simulated and laid out individually before being incorporated into the pixel array. While final transistor sizings may be different, the overall architecture remained the same. Both the pulse generator (II.b) and the pulse counter (II.a) were written in SystemVerilog and synthesized to create the layout of digital objects. The final pixels were fully integrated with all relevant blocks prior to the creation of the whole chip.



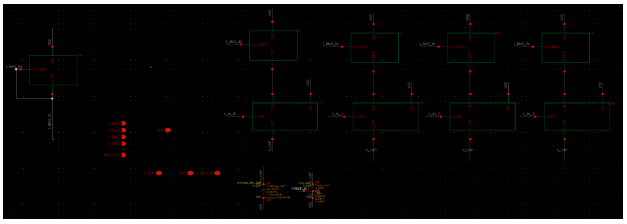
(a)



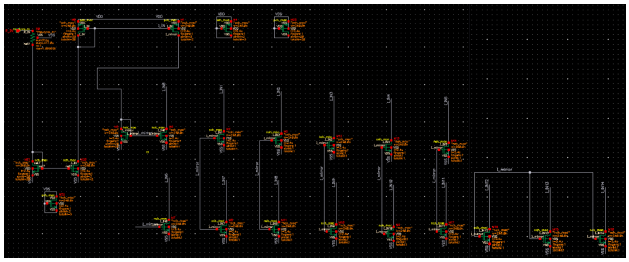
(b)



(c)



(d)



(e)

FIGURE II

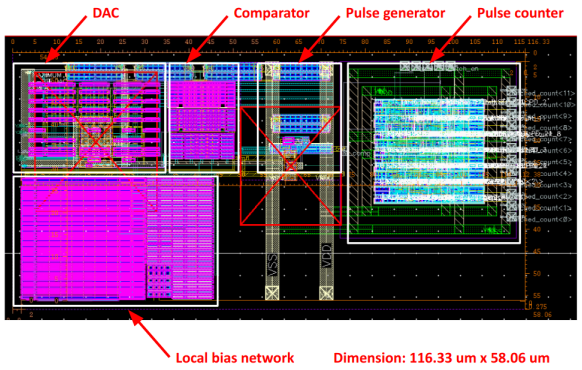
SCHEMATICS SCREENSHOTS: TOP LEVEL OF A PIXEL (a), COMBINED DAC ADC AND PULSE GENERATOR (b), ADC (COMPARATOR) (c), CURRENT DAC (d), (e) GROUP BIAS NETWORK

To provide a 100 nA bias current for the DAC and ADC of each pixel, a group bias network (II.e) consisting of a resistor-based current generation circuit and scaled-down current mirrors is also designed to scale down a 100 µA external reference current input generated from a potentiometer on the board level.

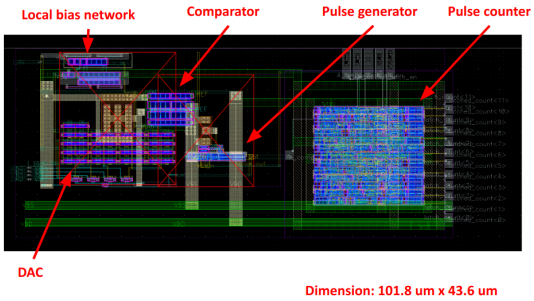
A final schematic was generated as part of the place and route (P&R) flow for the whole chip integration. This is where the scan chains for input and output are integrated.

B. Layout

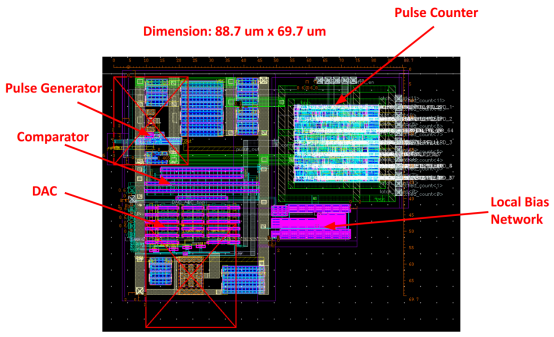
As with the schematics, the layout of each individual block was sectionalized to create a scalable and modular design that was easier to implement. Dimension of the combined pixel design was minimized as best as possible with each design. In addition, to improve the matching of our layout design, techniques such as common centroid layout are applied and dummy devices are placed around functional devices to increase the process uniformity and symmetry in our layout design. The same principle was also applied to the layout design of the group bias network.



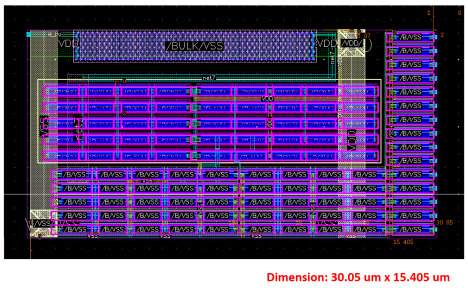
(a)



(b)



(c)



(d)

FIGURE III

INDIVIDUAL PIXEL AND GROUP BIAS NETWORK LAYOUTS WITH LABELS: PIXEL 1 (a), PIXEL 2 (b), PIXEL 3 (c), GROUP BIAS NETWORK (d)

C. Individual Pixel Simulation

DAC Inputs	Pixel 0 Count (tt @25C)	Pixel 1 Count (tt @25C)	Pixel 2 Count (tt @25C)	Pixel 3 Count (tt @25C)	Pixel 4 Count (tt @25C)
0000	0	0	0	0	0
0001	13	13	13	13	13
0010	24	24	24	24	24
0100	40	40	40	40	40
1000	77	77	77	77	77
1111	137	136	137	137	137

(a)

VIN	Pixel 0 Count (tt @25C)	Pixel 1 Count (tt @25C)	Pixel 2 Count (tt @25C)	Pixel 3 Count (tt @25C)	Pixel 4 Count (tt @25C)
0000	0	0	0	0	0
0001	58	58	58	58	58
0010	89	89	89	89	89
0100	104	104	104	104	104
1000	112	112	112	112	112
1111	118	118	118	118	118

(b)

DAC Inputs	Pixel 0 Count (tt @25C)	Pixel 1 Count (tt @25C)	Pixel 2 Count (tt @25C)	Pixel 3 Count (tt @25C)	Pixel 4 Count (tt @25C)
0000	0	0	0	0	0
0001	12	12	12	12	12
0010	22	22	22	22	22
0100	42	42	42	42	42
1000	81	81	81	81	81
1111	142	142	142	142	142

(c)

FIGURE IV

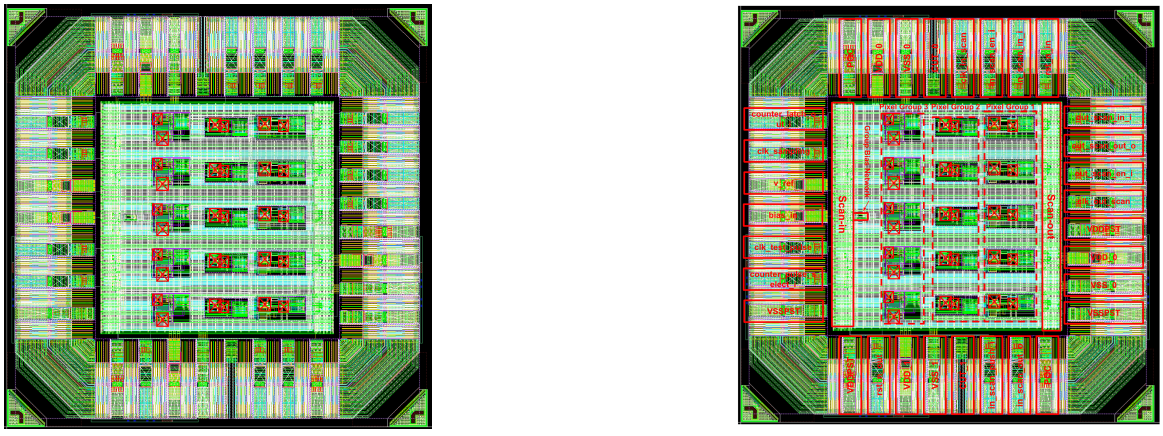
PIXEL TYPE 1 GROUP RESULTS (a), PIXEL TYPE 2 GROUP RESULTS (b), PIXEL TYPE 3 GROUP RESULTS (c)

Each pixel type shows a relatively linear relationship between VIN and the latched count which is as expected. Pixel type 2 does have a strong discontinuity between the max and min input values but mid-range values are not impacted despite their higher values. This linearity is shown better in Figure VI.c where the counter output is plotted.

D. Chip Integration and Layout

The whole chip layout was done using an Innovus flow to P&R each of the individual blocks. The die area is $1mm^2$ with a 5x3 pixel array, scan chain in and out, and the group bias. Any space where these blocks did not occupy were filled with decoupling capacitors and dummies to meet density requirements. Any remaining DRC errors were acceptable to be waived as per TSMC's design rules. The final layout is also LVS clean and has been simulated to ensure functionality. Simulation results can be found in the next section.

The layout of the individual blocks and pins were done in a linear fashion to allow for a reduction in longer signal paths or complicated routing. The power and ground pins are evenly spaced around the chip to ensure minimal resistive losses and power is distributed evenly through a large grid pattern on the higher layers (M8 and M9) of the chip. The scan-in and out circuits are synthesized on the left and right edges of the core with a width of 40 µm. Data on the chip flows from left to right starting out with the input scan chain. This forwards a specified input to a pixel DAC. This input is then processed for a set time period before the output scan chain reads the data from the pixel.



(a) (b)

FIGURE V

FULL CHIP LAYOUT (a) WITH LABELED PINS AND OTHER BLOCKS (b)

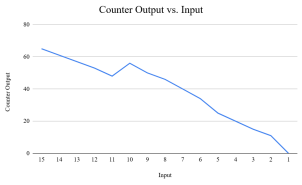
III. Whole Chip Simulation

Post-layout simulations show a relatively linear relationship between VIN and counter output on a per-pixel type level. This reinforced the simulation trends from the individual pixel results though the actual counter outputs are not identical to those tests.

Across pixel types, there is not as strong of a linear relationship between VIN and counter output. This is down to the differences in design specifications for each pixel.

Pixel #	Input	Counter Output	**Pixel #**	Input	Counter Output	**Pixel #**	Input	Counter Output
0	15	65	**5**	10	56	**10**	5	25
1	14	61	**6**	9	50	**11**	4	20
2	13	57	**7**	8	46	**12**	3	15
3	12	53	**8**	7	40	**13**	2	11
4	11	48	**9**	6	34	**14**	1	0

(a)



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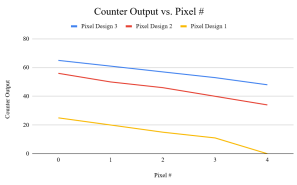

(c)

FIGURE VI

PIXEL GROUP RESULTS TABLE (a), RESULTS FROM EACH INDIVIDUAL PIXEL FROM VI.a (b), RESULTS FROM EACH PIXEL TYPE FROM VI.A (c)

IV. Performance Summary

Technology	TSMC 65nm
Die Area	1mm x 1mm
Core Area	554µm x 556µm
Core Supply Voltage	1.2V
Type 1 Single Pixel Area	6754.12 μm^2
Type 2 Single Pixel Area	4110 μm^2
Type 3 Single Pixel Area	6182.39 μm^2
Group BiasNetwork Area	462.92 μm^2
Total Pxiel Number	3x5
DAC Resolution	4-Bit
DAC Voltage Ramping Rate	~1V/1µs
Comparator Response Time	<17.33ns
Pulse Counter Resolution	12-Bit

FIGURE VII

CHIP PERFORMANCE SUMMARY

Overall, the performance of our individual blocks and the whole chip all satisfies or exceeds our target specifications while there remains room for improvement.

V. Design Optimization

Much of the optimization for this chip would be done at an individual block level. In layout design, some areas in pixel designs lack dummy transistors to improve performance and matching between elements. Open areas among each of the pixel blocks could have been filled with decoupling capacitors which would improve power supply stability and noise characteristics at a local level. The performance of each group member's pixel design can also be fine-tuned to have a more uniform performance and improve the output linearity.

On the chip level, one major design optimization that can be conducted is to make sure all of the reserved upper layer power rails inside of the individual pixels can be fully aligned and connected to the vertical power grid of the chip by defining a custom routing scheme for better power distribution. The placement of the group bias network may also be improved by placing it in the middle of the core instead of the left-hand side of the core so that the bias voltage can be more equally distributed to all pixels and less affected by the IR drop caused by longer traces.

Mutual Grading

This section will consist of the grading from each group member. Each section is written by the person whose name is before the colon.

Alec: Kaiyuan and Rylan were great partners throughout the process of the project. We communicated and did work efficiently together as a team, and ensured no one was left behind in the tapeout flow. Overall, it was a great effort between the three of us that contributed to our overall success.

Kaiyuan: Alec and Rylan were great teammates on this project. All of us contributed evenly, ensuring tasks were completed efficiently and effectively. Communication was always clear and collaborative, which made the entire tapeout process smooth and successful.

Rylan: Both Alec and Kaiyuan were excellent partners for this project. We each shared the work evenly and all parts were completed in a timely manner. There was no time where it felt like we were being held up due to something not being done. Most of the chip integration and simulation was done together in HH-1305 so we were all able to be very hands on with the tapeout flow.