CLOCK TOPOLOGY CURATION AND ANALYSIS

Potential for Better Clock Trees

- Clock team's current design uses tried and true methodologies
- Curate new clock tree topologies and analyze their efficacy
- Compare and contrast current vs curated clock tree designs

Clock Mesh Overview

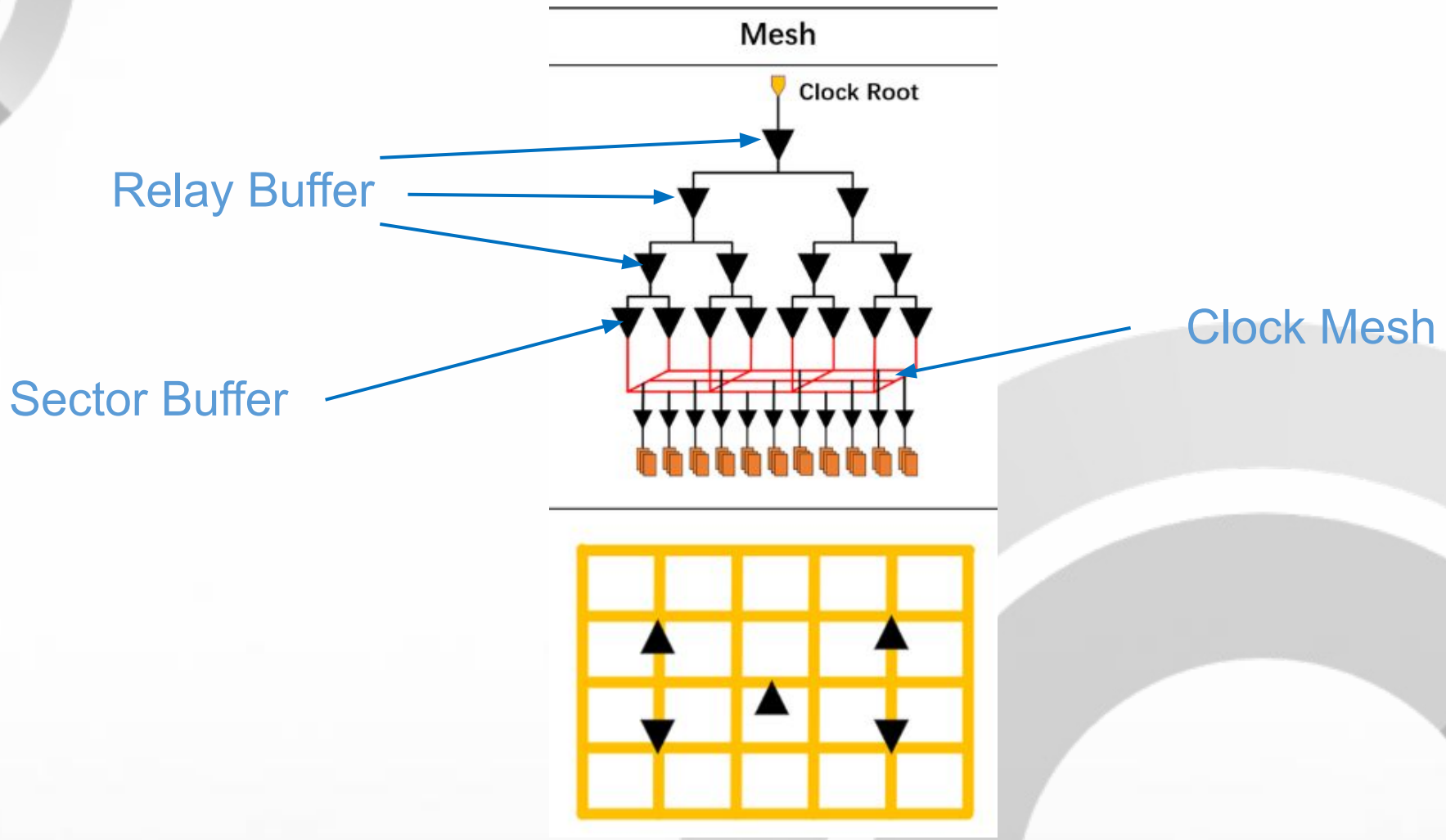


Figure 8: VLSI Korea, Clock Tree Mesh Structure

Clock Mesh From IBM Perspective

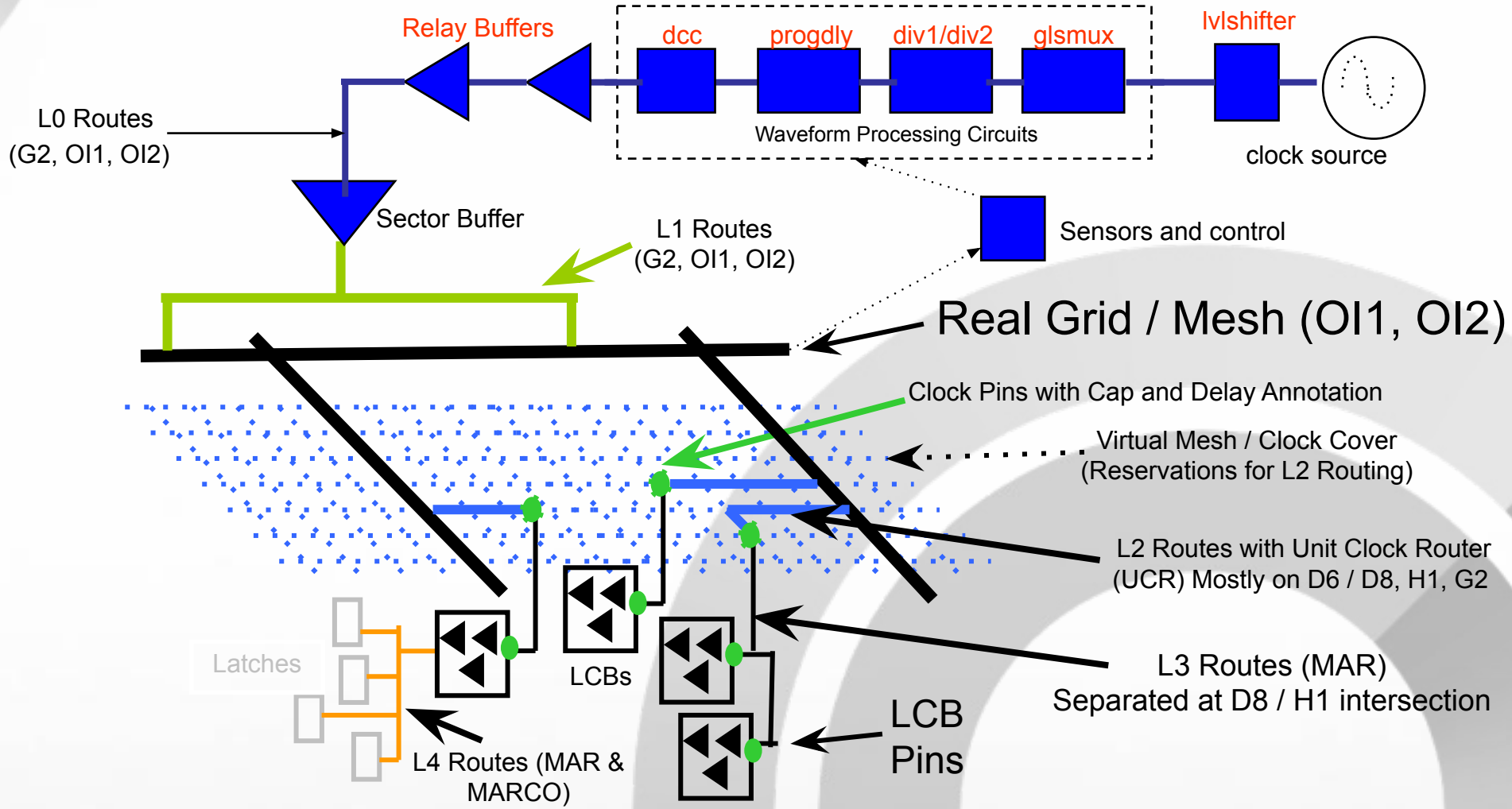


Figure 9: Eric Lai, Clocking naming Convention, PD Infrastructure – Clocking Overview

Clock Mesh From IBM Perspective

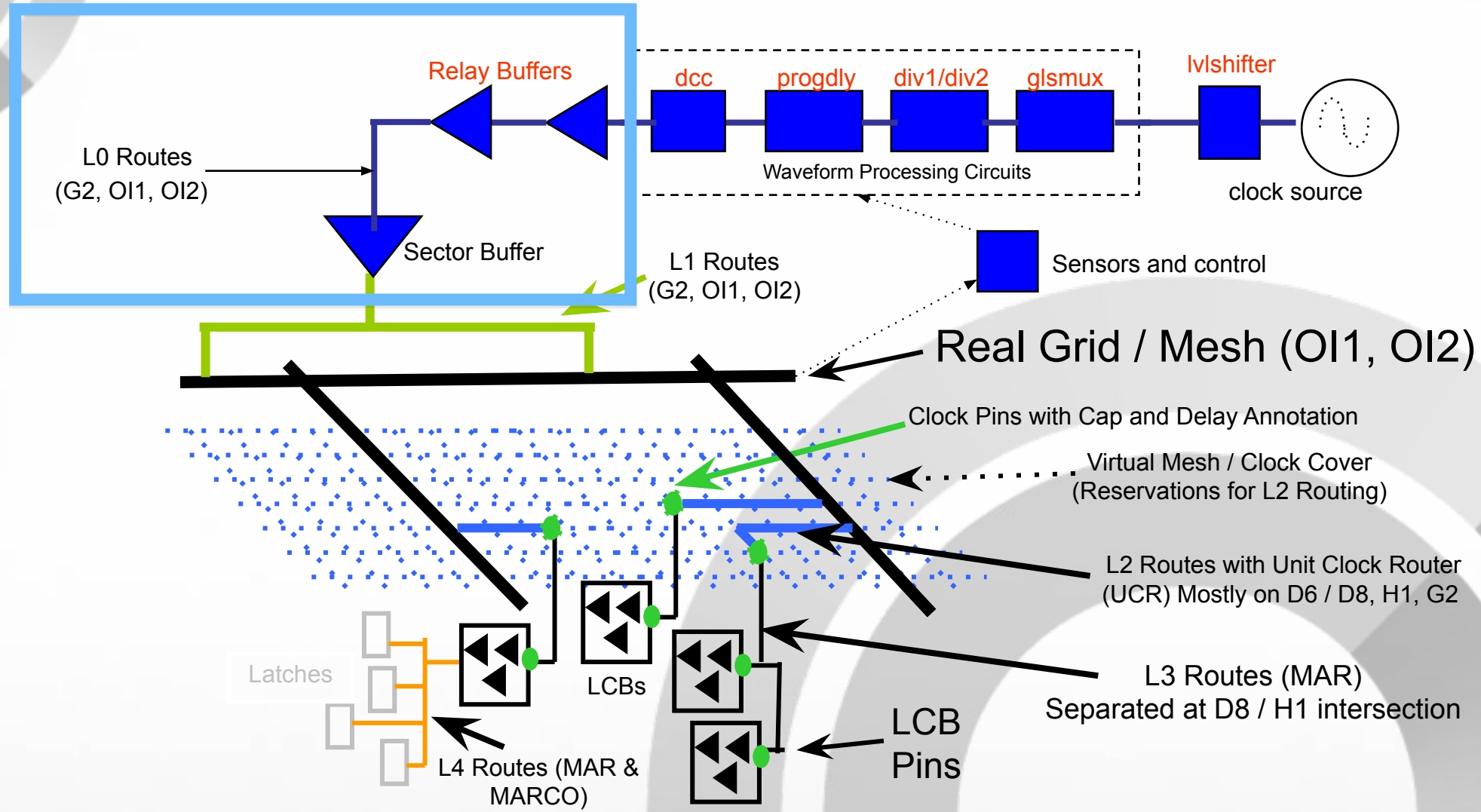


Figure 9: Eric Lai, Clocking naming Convention, PD Infrastructure – Clocking Overview

General Tree Topology Differences

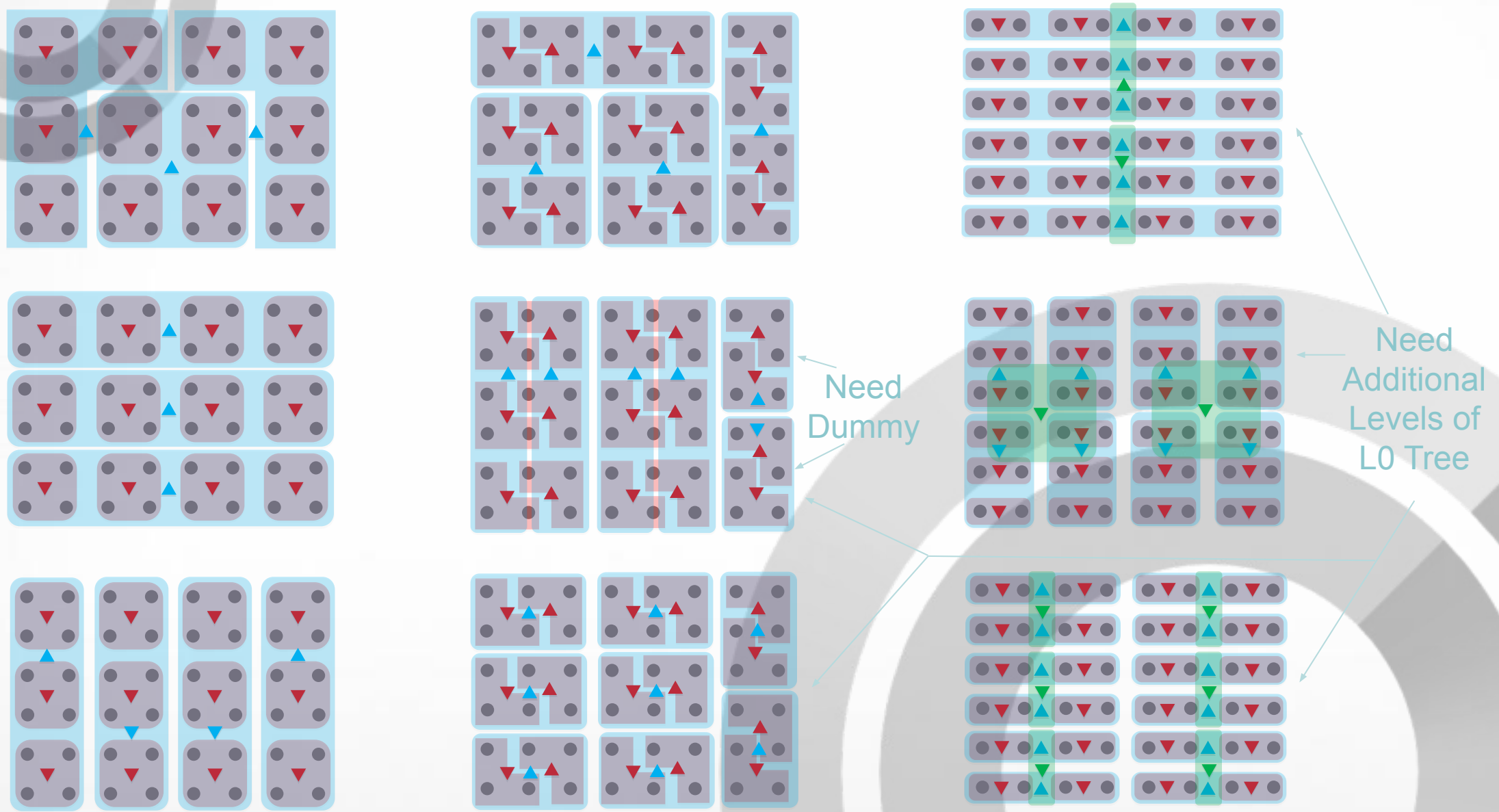


Figure 10: Eric Lai, Potential Clock Tree Structures

Initial Topology

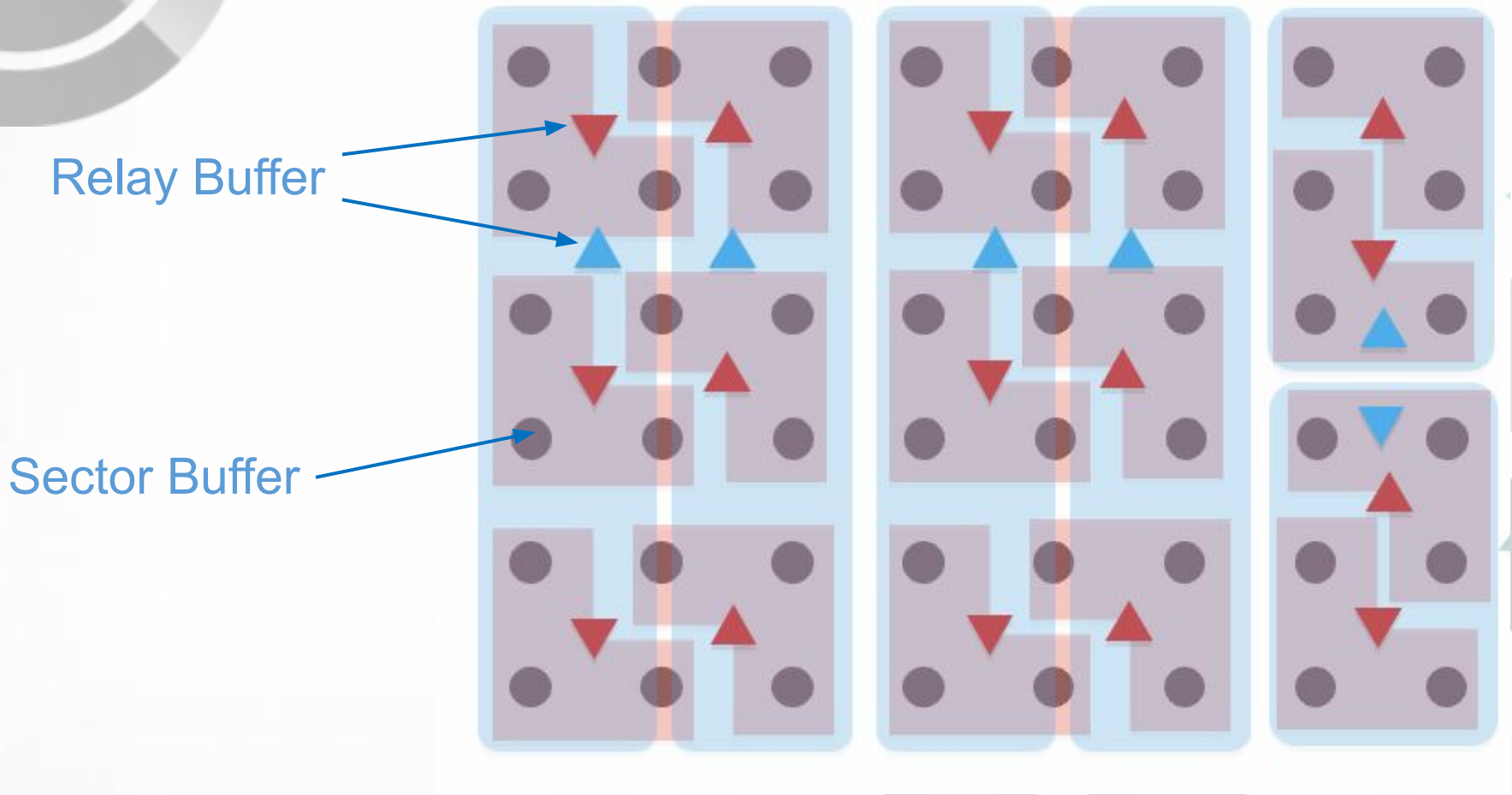


Figure 11: Eric Lai, Potential Clock Tree Structures, Topology #5

Blank Relay & Buffer Layout

Relay Buffer

Sector Buffer

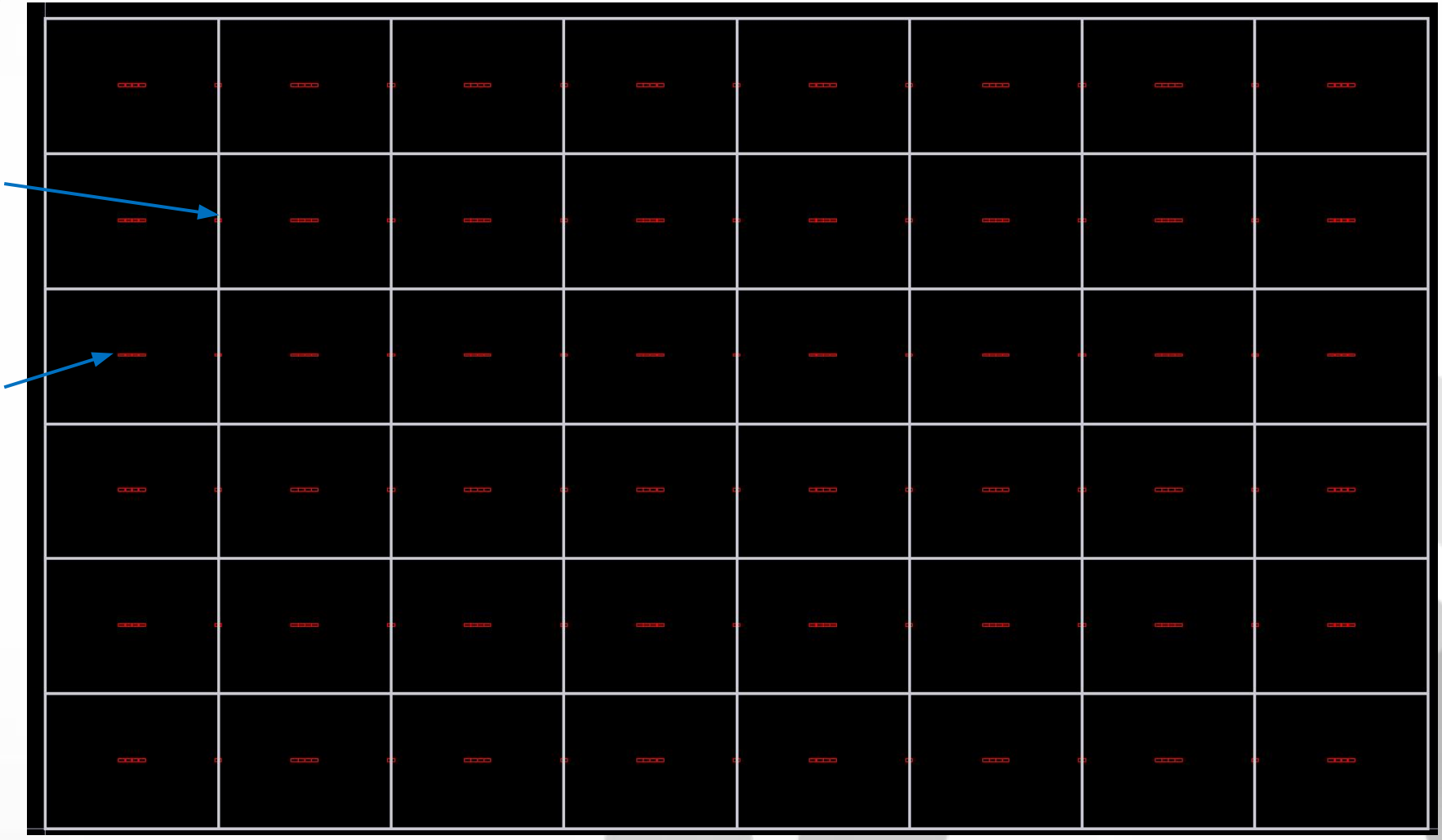


Figure 12: Alec Bender, Blank Relay & Buffer Layout

Connected Relay & Buffer Layout

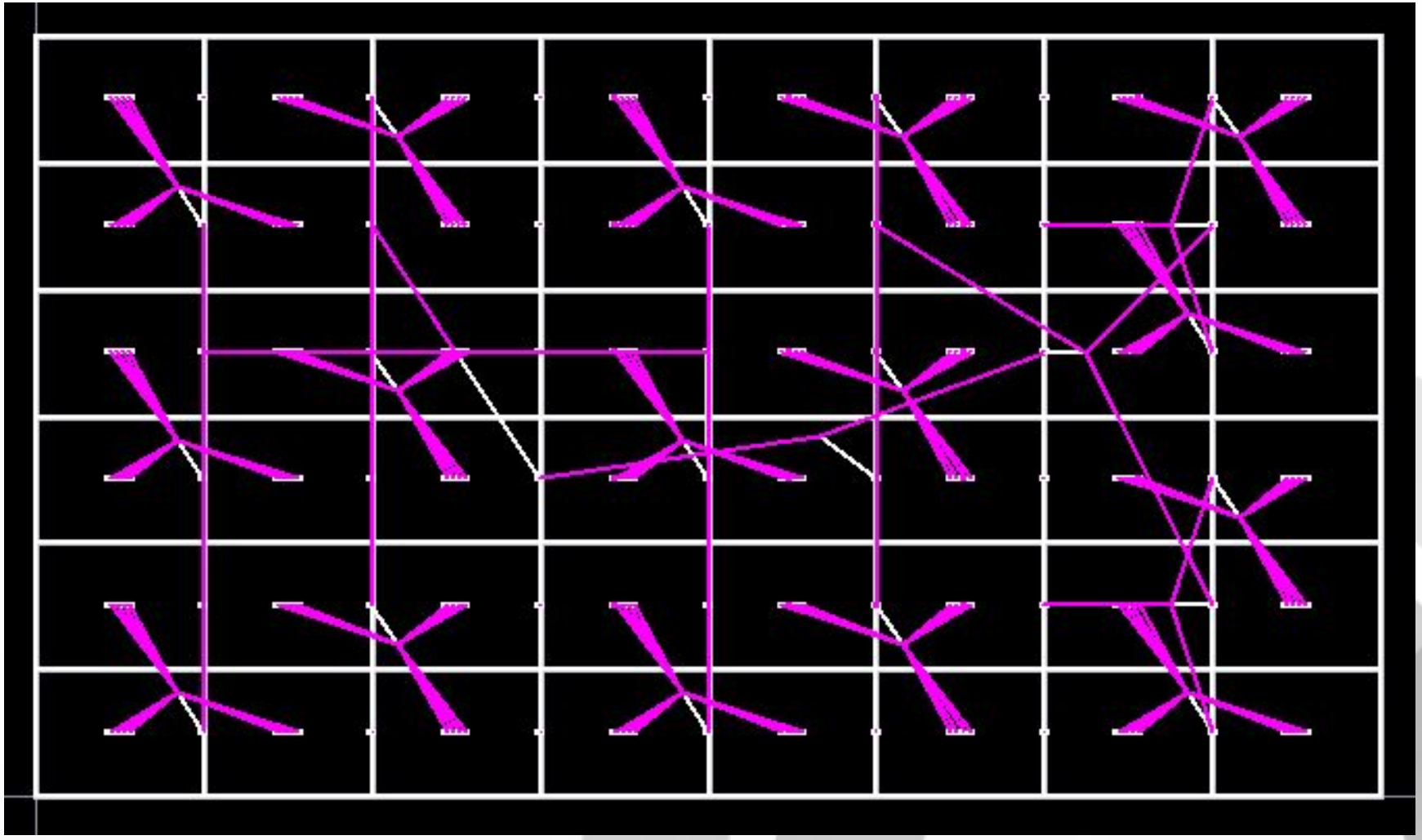


Figure 13: Alec Bender, Connected Relay & Buffer Layout

Wired Relay & Buffer Layout

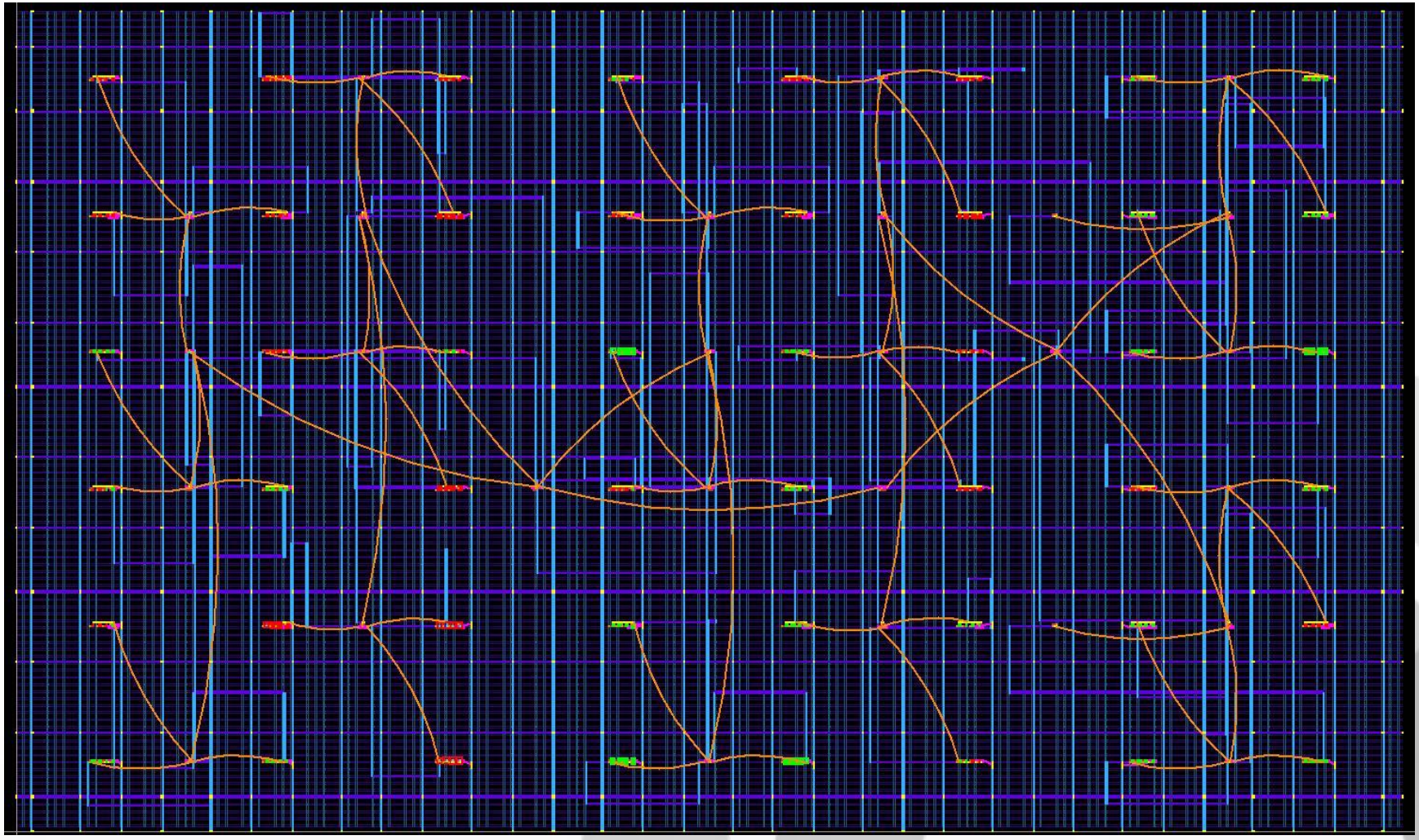


Figure 14: Alec Bender, Wired Relay & Buffer Layout

Testing Metrics

- Max Slew (signal change over time)
- Max Skew (difference in arrival times)
- Mean Arrival Time
- Power
- Routability
- Distances and Fanout (connections from output)

Clock Tree Metric Output

Clock Tree Layer

Slew, under 25ps

```
MeasSum  m=  9 ntot= 192 SKEW= 2.0 SLEWM=  23.2 DUTY= 0.500 UM=   2 OM=  -4 SWM= 0.693 time= 153.6 tmin= 152.5 tmax= 154.4 slewMin=22.2 slewMax=24.1 slewR= 2.0 Umin=   0 Umax=   3 Omin=  -5 Omax=   0 dutyMin= 0.499 dutyMax= 0.500
MeasSum  m= 11 ntot=  16 SKEW= 1.6 SLEWM=  18.0 DUTY= 0.509 UM=   0 OM=  -2 SWM= 0.697 time= 112.9 tmin= 112.1 tmax= 113.7 slewMin=17.4 slewMax=18.5 slewR= 1.1 Umin=  -1 Umax=   2 Omin=  -3 Omax=   0 dutyMin= 0.509 dutyMax= 0.509
MeasSum  m= 13 ntot=   6 SKEW= 1.1 SLEWM=  19.8 DUTY= 0.501 UM=  -2 OM=   2 SWM= 0.705 time=  75.0 tmin=  74.5 tmax=  75.6 slewMin=19.3 slewMax=20.2 slewR= 0.9 Umin=  -3 Umax=  -1 Omin=   2 Omax=   3 dutyMin= 0.501 dutyMax= 0.501
MeasSum  m= 15 ntot=   2 SKEW= 0.9 SLEWM=  15.1 DUTY= 0.507 UM=   0 OM=   0 SWM= 0.699 time=  33.3 tmin=  32.8 tmax=  33.8 slewMin=14.9 slewMax=15.3 slewR= 0.4 Umin=  -1 Umax=   1 Omin=  -1 Omax=   1 dutyMin= 0.507 dutyMax= 0.507
MeasSum  m= 17 ntot=   1 SKEW= 0.0 SLEWM=  11.9 DUTY= 0.500 UM=   0 OM=   0 SWM= 0.700 time=   0.0 tmin=   0.0 tmax=   0.0 slewMin=11.9 slewMax=11.9 slewR= 0.0 Umin=   0 Umax=   0 Omin=   0 Omax=   0 dutyMin= 0.500 dutyMax= 0.500
MeasSum  m=211 ntot=   2 SKEW= 0.3 SLEWM=  16.1 DUTY= 0.509 UM=   2 OM=  -4 SWM= 0.692 time= 112.9 tmin= 112.8 tmax= 113.1 slewMin=16.1 slewMax=16.1 slewR= 0.0 Umin=   0 Umax=   2 Omin=  -4 Omax=   0 dutyMin= 0.509 dutyMax= 0.509
OPT1 targ=  62 skew=1022.0 mean=  207.1 early=    0.0 late=1022.0 ttmin=   11.9 ttmax= 1550.0 loadC=  0.00 wireC= 31.73 totC=  31.7 CV2F= 62.2 totP= 113.3 Uplift=1.8214
DONE S10L0filtSpider: (atbender.29Jul24.16:23:34) completed SUCCESSFULLY:
```

Skew, under 4ps

Arrival Time, optimize

Total Power, optimize

*All other metrics within spec
**Feq = 4GHz, VDD=0.7

Figure 15: Alec Bender, summary

Clock Tree Analysis Part 1

Utilizing spider2 significantly decreases power and time for FO4

Topology	totP (mW)	Percent Inc	slewMax	SLEWM	time (ps)	SlewMax Level	FO (m=11)	FO (m=13)	FO (m=15)	FO (m=17)	FO (m=19)
1	78.00	1.00	23.50	23.10	120.00	9	4	4	3		
2	84.49	1.08	25.40	24.30	118.10	9	4	4	3		
3	83.32	1.07	24.70	24.20	118.40	9	4	3	4		
4	111.80	1.43	23.80	23.40	126.80	13	3	4	4		
5	113.30	1.45	24.10	23.20	153.60	9	3	3	3	2	
6	109.80	1.41	24.20	23.20	151.00	9	3	2	3	3	
7	104.20	1.34	24.80	24.60	149.70	13	2	4	3	2	
8	92.20	1.18	21.90	21.50	145.70	13	2	2	4	2	
9	105.00	1.35	24.50	23.40	168.40	15	2	2	2	3	2

Multiple FO2, deeper clock trees consumes less power than FO3

Figure 16: Alec Bender, Clock Tree Analysis Summary

Spider2 Explanation

Figure 17: Alec Bender, Spider2

Clock Tree Topology #10

10.1

- Lower power buffers

10.2

- Higher power buffers

10.3

- Without Spider2

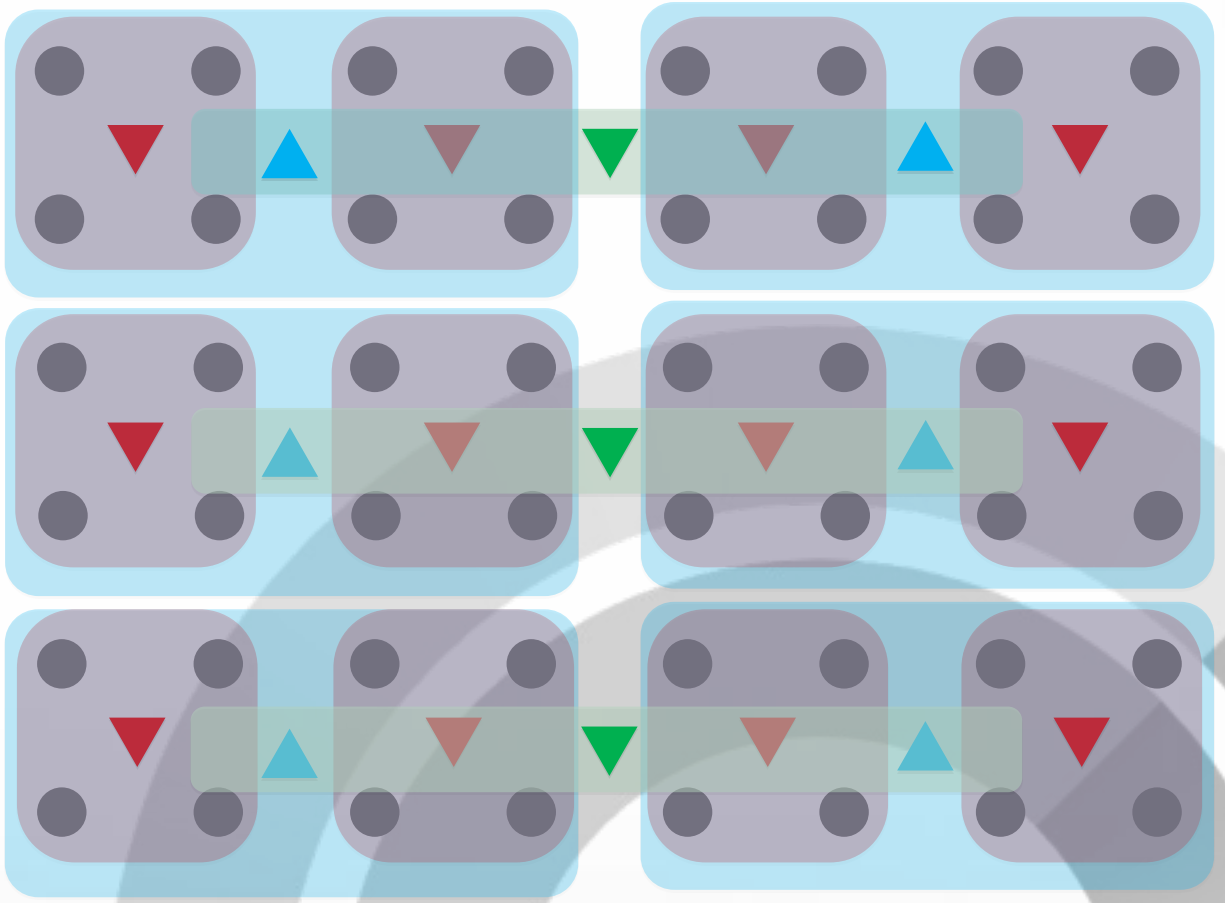


Figure 18: Alec Bender, clock topology #10

Clock Tree Analysis Part 2

Replacing FO4, FO3 directly with multiple FO2 trades off a slight power decrease for time

Topology	totP (mW)	Percent Inc	slewMax	SLEWM	time (ps)	SlewMax Level	FO (m=11)	FO (m=13)	FO (m=15)	FO (m=17)	FO (m=19)
1	78.00	1.00	23.50	23.10	120.00	9	4	4	3		
2	84.49	1.08	25.40	24.30	118.10	9	4	4	3		
3	83.32	1.07	24.70	24.20	118.40	9	4	3	4		
4	111.80	1.43	23.80	23.40	126.80	13	3	4	4		
5	113.30	1.45	24.10	23.20	153.60	9	3	3	3	2	
6	109.80	1.41	24.20	23.20	151.00	9	3	2	3	3	
7	104.20	1.34	24.80	24.60	149.70	13	2	4	3	2	
8	92.20	1.18	21.90	21.50	145.70	13	2	2	4	2	
9	105.00	1.35	24.50	23.40	168.40	15	2	2	2	3	2
10.1	81.8	1.05	25.70	25.20	141.40	9	4	2	2	3	
10.2	82.44	1.06	24.60	24.20	127.50	9	4	2	2	3	
10.3	89.48	1.15	30.50	29.50	130.20	9	4	2	2	3	

Even a slight trade off for power (more powerful buffers) can significantly decrease time

Figure 19: Alec Bender, Clock Tree Analysis Summary

Future Steps

Compare curated topologies with lower tracks

- See how successful curated topologies and fan outs are with less available tracks

Compare significantly high fanouts

- Test FO5, FO6 with Spider2 to see if they would meet spec

Take results into consideration for current and future projects

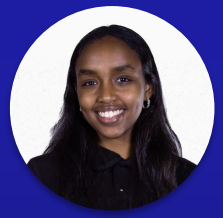
- Minimize usage of FO3 near the sector buffers in favor FO2/FO4

PROJECT OVERVIEW

Lessons and Skills Learned

- Pandas
- JSON
- openpyxl, xlsxwriter
- MongoDB
- Clock Tree Synthesis
- Timing Metrics
- Synopsys EDA

Acknowledgements



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Questions