Gate Stack: Demo 3

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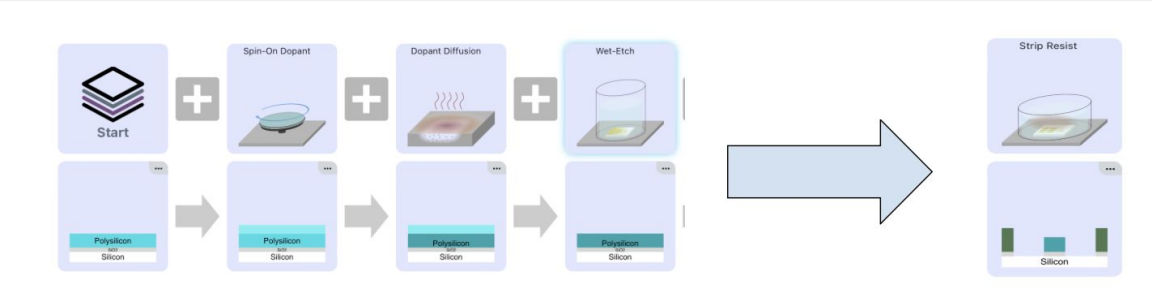
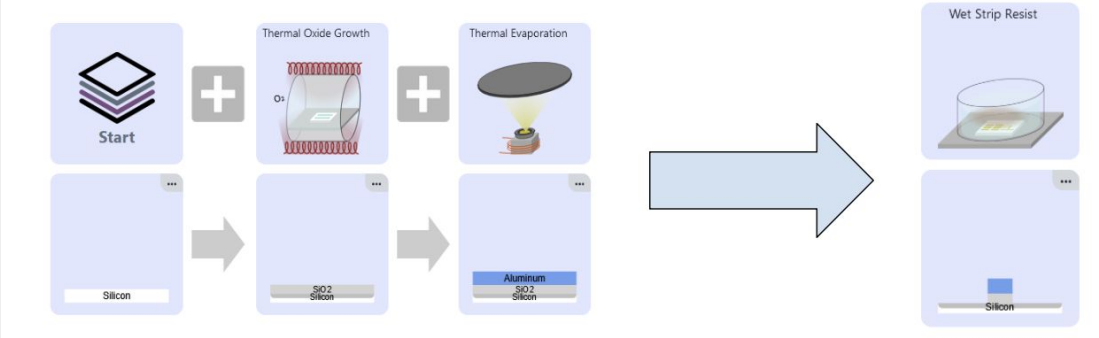
Explanation of the Project

Goal

Make our own gate stack as a replacement for the current pre-deposited polysilicon



Current gate stack process (300nm P-doped polysilicon, 20nm SiO2)



Desired gate stack process (~500nm Al, ~30nm SiO2)

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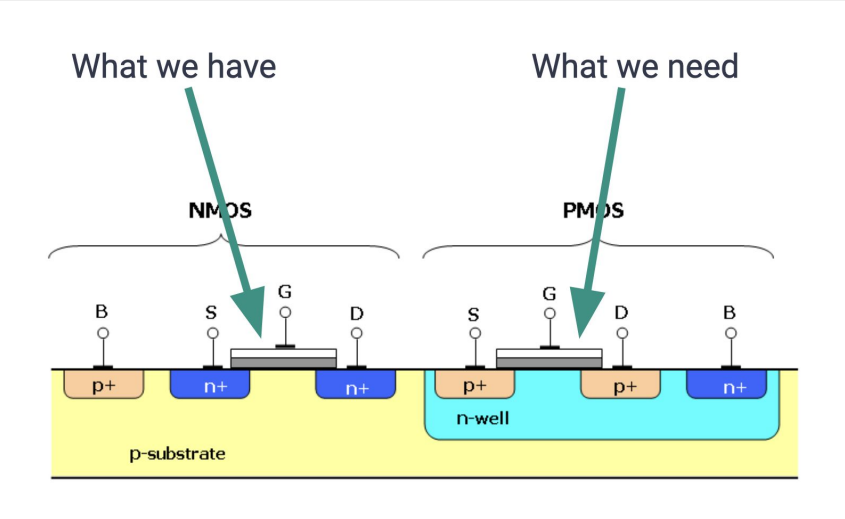
Reasoning

1. Gate stack blocks doping n-well into silicon for PMOS development
2. full control of the entire stack of the transistor from bare silicon



NMOS (left), PMOS (right). Gate stack blocks n-well deposition

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What is the Gate Stack

- Determines the threshold voltage (Vth) of the transistor
  - The voltage required to turn the transistor on
  - The thickness and material of the gate dielectric can affect the Vth and the overall performance of the transistor

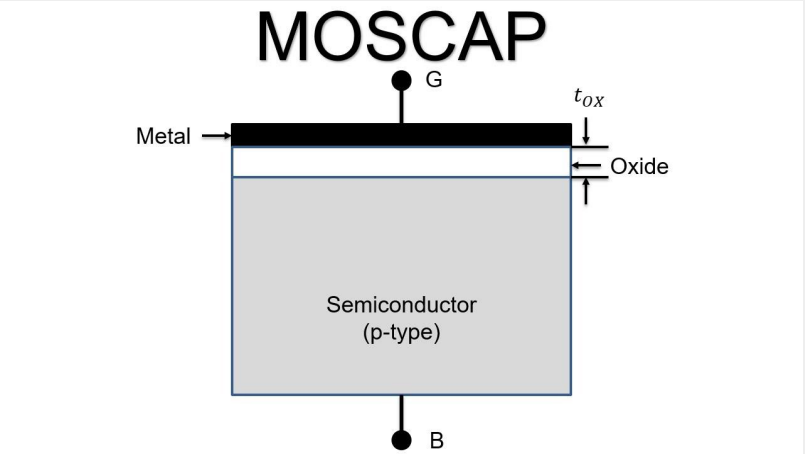

Diagram of a MOSCAP (Metal-Oxide Semiconductor Capacitor) consisting of a Metal (typically Al), Insulator (typically SiO2), and semiconductor (P or N type doped Si)

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Recap: Demo 1 and Demo 2

Batch V0

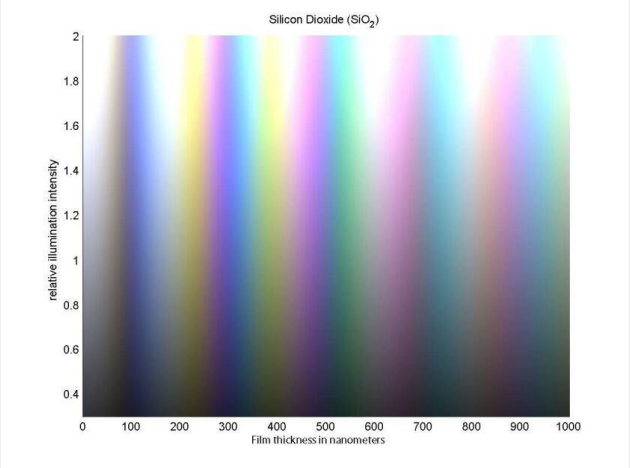
Chip 326: 1100˚C, 5 min
Chip 327: 1100˚C, 15 min
Chip 332: 1100˚C, 30 min
Chip 333: 1100˚C, 60 min
Chip 334: 1100˚C, 120 min

Goal:

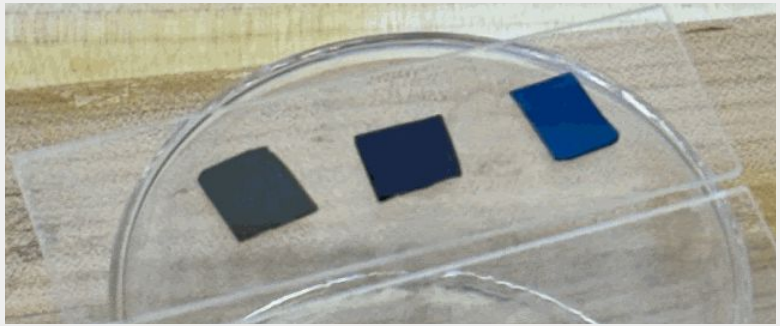
- Characterize the oxide growth rate of the tube furnace

Result:

- Visual inspection of thickness would not suffice
  - Must find a better method
- From initial batch, anything over 60min is well beyond 100nm range



SiO2 thickness chart



Chips 332-334 (left to right)

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Batch V1

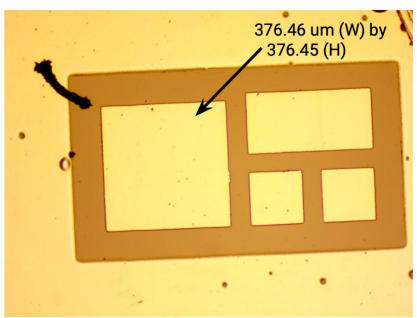
Chip 392: 1100˚C, 2 min
Chip 393: 1100˚C, 4 min
Chip 394: 1100˚C, 6 min
Chip 395: 1100˚C, 8 min
Chip 396: 1100˚C, 10 min
Chip 397: 1100˚C, 2 min; Al deposition
Chip 398: 1100˚C, 4 min; Al deposition
Chip 399: 1100˚C, 6 min; Al deposition
Chip 400: 1100˚C, 8 min; Al deposition
Chip 401: 1100˚C, 10 min; Al deposition

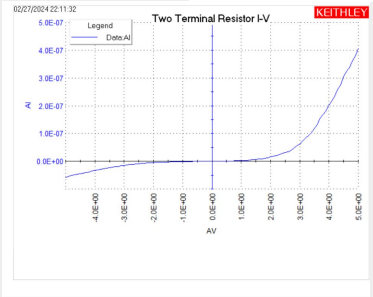
Goal:

- Find ideal time to grow 20nm oxide
- Find oxide thickness for ideal electrical characteristics

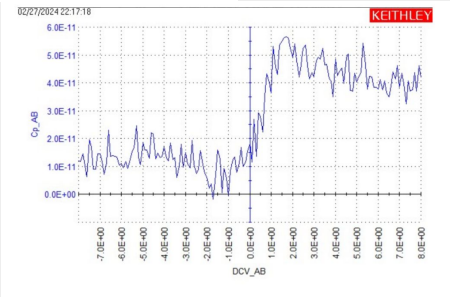
Result:

- Reflectometer showed ~25-46nm thickness
- ∴ Need to lower tube furnace temp





IV Curve



CV Curve

Chips 392-396 (left to right)

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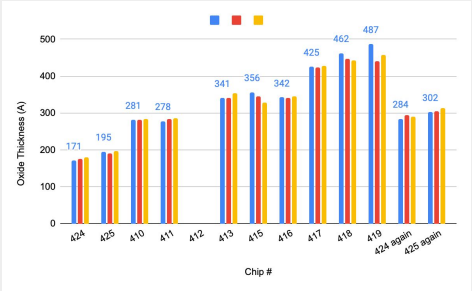
Batch V2

Chip 410, 411, 412: 1000˚C, 10 min
Chip 413, 415, 416: 1050˚C, 10 min
Chip 417, 418, 419: 1100˚C, 10 min
Chip 424, 425, 436, 437: 20nm Polysilicon as is



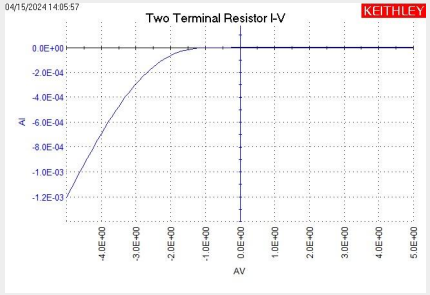
Reflectometer Data

Goal:

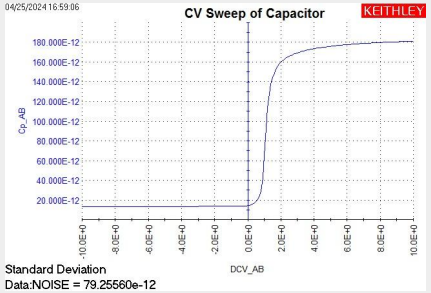
- Characterize oxide growth and electrical properties at lower temp compared to 1100˚C and as-is polysilicon

Result:

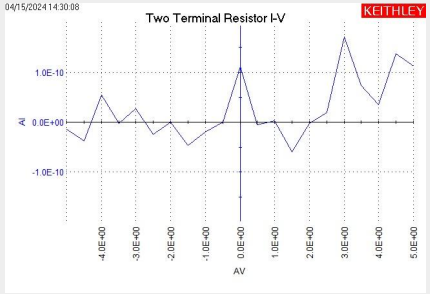
- Demo chip contaminated due to unclean environment
- ∴ higher voltage threshold due to inherent defects and contaminants
  - Vth went down over subsequent tests
  - Fixed charges stay within oxide, requiring less voltage



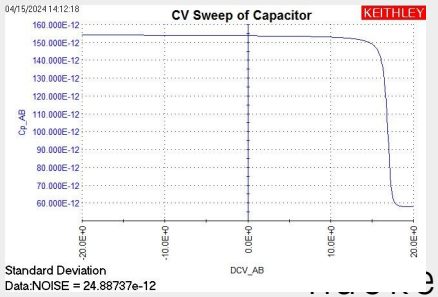
Chip 424 Ground Truth IV



Chip 436 Ground Truth CV



Chip 418 Demo IV



Chip 418 Demo CV

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Batch V3

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Goal

- Explore methods for less contaminants
- Two ways to problem solve
  - Oxide deposition method is deposited/grown cleanly
  - Make thermal oxidation inherently “clean”

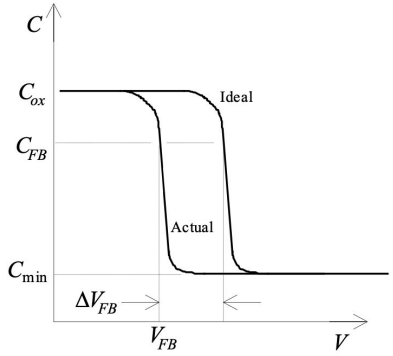

Fig. 44: Flat band shift due to oxide fixed charge (*p*-type substrate; accumulation at left)

Fixed charges mainly arise from mobile ion contamination ∴ resulting in a band shift

Capacitance-Voltage Measurement, Portland State University

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Reasonable Clean Oxide Deposition Methods

- High Temp Plasma Oxide Growth
  - High temperature (300-600˚C)
- Plasma-Enhanced Chemical Vapor Deposition (PECVD)
  - Use a silicon precursor (i.e. TMOS, TEOS, HDMSO) with an oxidizer
- Sputtering
  - Instead of growing the oxide, pure SiO2 is deposited onto the surface of the silicon chip
- Low Temp Plasma Oxide Growth
  - Low temperature (20˚C)

Reasonable Clean Oxide Deposition Methods

- High [illegible] Plasma Oxide Growth
  - [illegible] Temperature ([illegible]C)
- Plasma-Enhanced Chemical Vapor Deposition (PECVD)
  - Use a silicon precursor (i.e. TMOS, TEOS, HDMSO) with an oxidizer
- Sputtering
  - Instead of growing the oxide, pure SiO2 is deposited onto the surface of the silicon chip
- Low Temp Plasma Oxide Growth
  - Low temperature (20˚C)

→ Plasma etcher not capable of high temperature environments

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Reasonable Clean Oxide Deposition Methods

- High [illegible] Plasma Oxide Growth
  - [illegible] temperature (300[illegible]C)
- Plasma-Enhanced Chemical Vapor Deposition (PECVD)
  - Use [illegible] precursor (i.e. TMOS, TEOS, HDMSO) with an oxidizer
- Sputtering
  - Instead of growing the oxide, pure SiO2 is deposited onto the surface of the silicon chip
- Low Temp Plasma Oxide Growth
  - Low temperature (20˚C)

Do not have precursors in the lab at the moment

More importantly, using deposition in the same machine for cleaning is not the best (precursor will stick to the walls of the chamber)

Reasonable Clean Oxide Deposition Methods

- High [illegible] Plasma Oxide Growth
  - [illegible] temperature ([illegible]°C)
- Plasma-Enhanced Chemical Vapor Deposition (PECVD)
  - Use [illegible] precursor (i.e. TMOS, TEOS, HDMSO) with an oxidizer
- Sputtering
  - Instead of [illegible] oxide, pure SiO2 is deposited onto the surface of the silicon chip
- Low Temp Plasma Oxide Growth
  - Low temperature (20˚C)

Do not have sputtering capabilities in the lab

→ This is planned to be a next semester project

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Reasonable Clean Oxide Deposition Methods

- High [illegible] Plasma Oxide Growth
  - [illegible] temperature (300˚C)
- Plasma-Enhanced Chemical Vapor Deposition (PECVD)
  - Use [illegible] precursor (i.e. TMOS, TEOS, HDMSO) with an oxidizer
- Sputtering
  - Instead [illegible] oxide, pure SiO2 is deposited onto the surface of the silicon chip
- Low Temp Plasma Oxide Growth
  - Low temperature (20˚C)

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Batch V3.1

434: Plasma Oxide Growth

Goal:

- Test low temperature plasma oxide growth

Result:

- Extremely low oxide growth
  - 434: ~9 nm
- This method was not going to be suitable for Hacker Fab

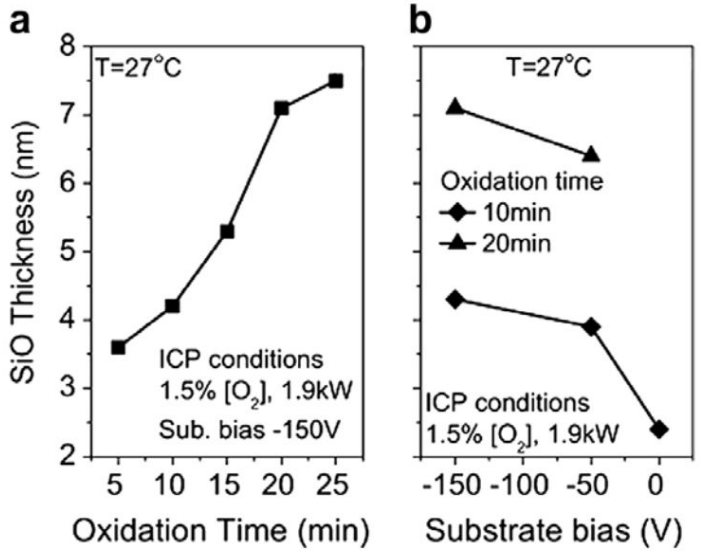

Fig. 1. Evolution of T_{OX} at room-temperature as a function of (a) PO time at fixed $V_{BS} = -150$ V and (b) V_{BS} for 10 min and 20 min PO times.

Low growth was expected

High-density plasma silicon oxide thin films grown at room-temperature, Institute of Microelectronics

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“Clean” Thermal Oxidation – RCA Clean

- Standard silicon wafer cleaning procedure
  - Organic clean
    - H202 and NH3 solution
    - Also can be substituted with plasma O2 clean
  - Oxide Strip
    - HF etch
  - Ionic clean
    - H202 and HCl solution
- Also added inclusion of HCl during oxidation for some chips
  - Getter and immobilize ionic contaminants during growth
    - Concentration of 0.0068% HCl (number stemmed from OSHA parameters)

Batch V3.2

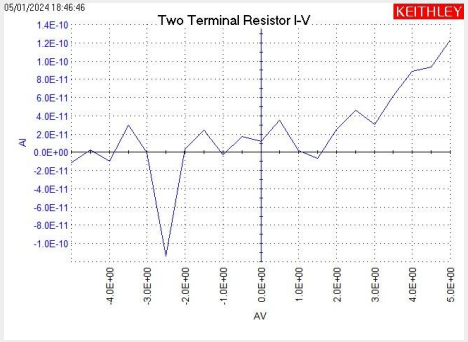
Chip 457: 1100˚C, 10min – Full RCA
Chip 458: 1100˚C, 10min – RCA w/ O2 clean
Chip 460: 1100˚C, 10min – Full RCA + HCl
Chip 461: 1100˚C, 10min – RCA w/ O2 clean + HCl
Chip 462: 1100˚C, 10min – HCl

Goal:

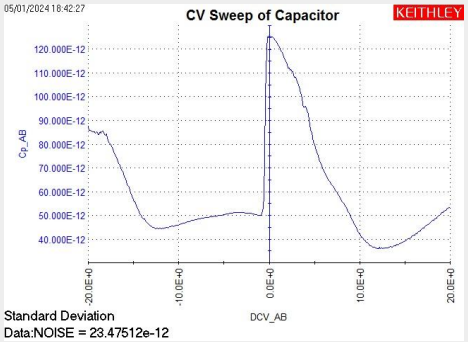
- Test RCA cleaning for thermal oxide growth

Results – non HCl

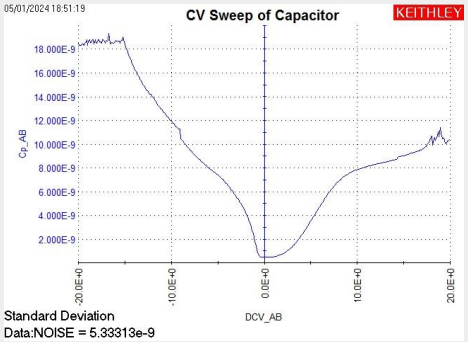
Chip 457 IV



Chip 458 IV



Chip 457 CV



Chip 458 CV

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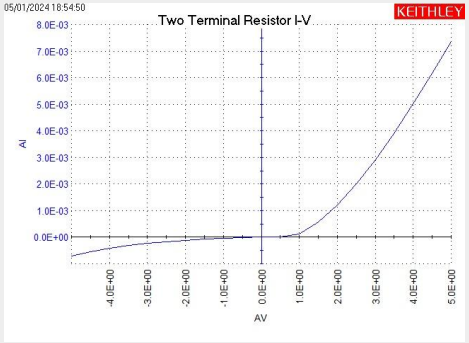
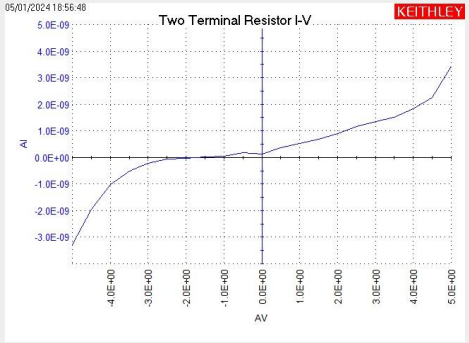
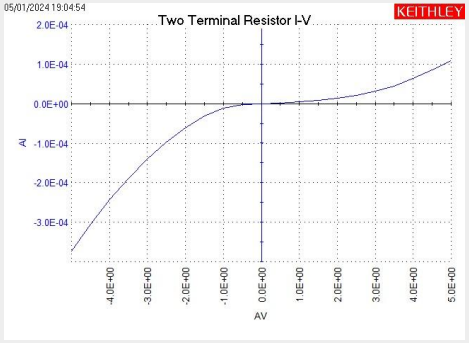
Results – HCl



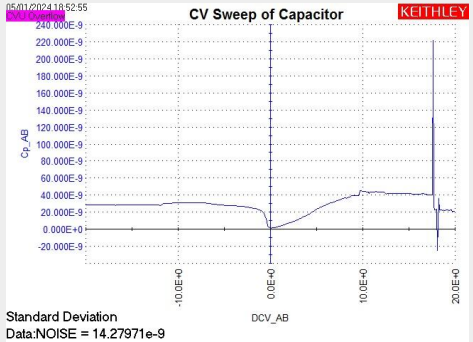
Chip 460 IV



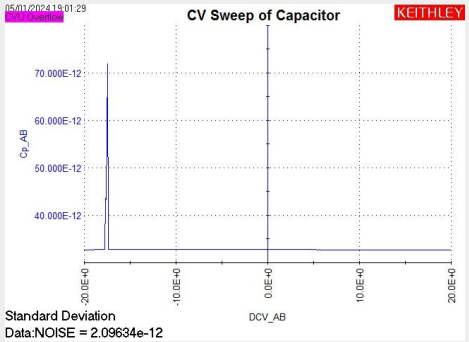
Chip 461 IV



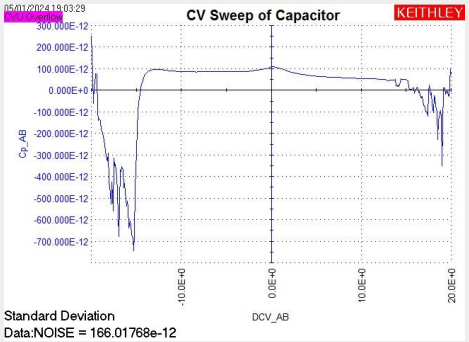
Chip 462 IV



Chip 460 CV



Chip 461 CV



Chip 462 CV

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Overall Results

	IV Curve	CV Curve
Non HCl	Insulating	Somewhat MOSCAP shape
HCl	Heavy leakage	Not MOSCAP shape

- The undesirable CV data is believed to have stemmed from unreliable CV data measurements or process variation rather than the RCA clean itself

Batch V2 Contamination Test

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Outline

1. Baseline CV Curve Test
2. Apply a large positive bias
   a. CV Test from 19-20V
   b. Heat substrate to 200˚C
      i. Sweep mobile ions in the oxide to the SiO2 interface
3. Substrate is cooled, bias is removed
   a. A translation of the CV curve indicates contamination

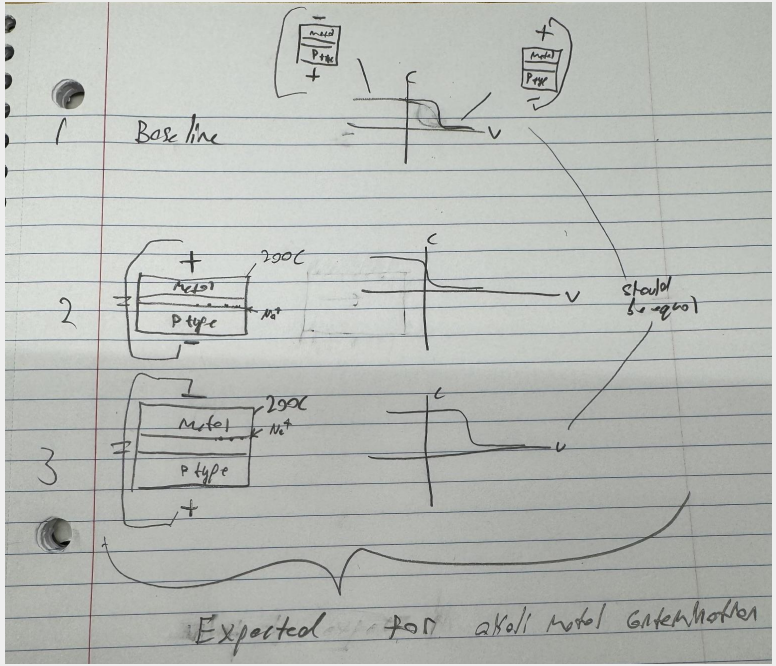

Illustration showing contamination steps test and effect on fixed charges

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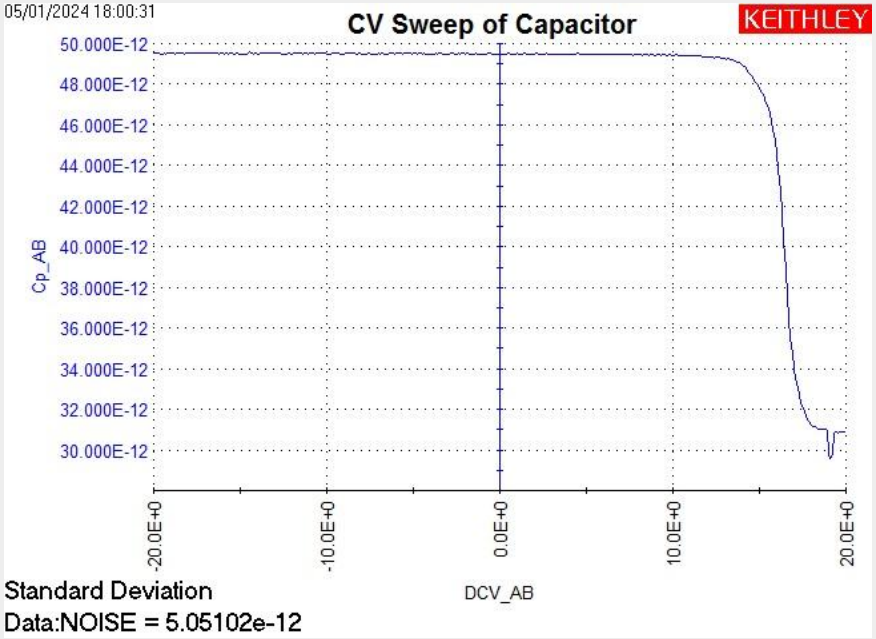
Baseline



Chip 417 CV Curve with Vth >15V

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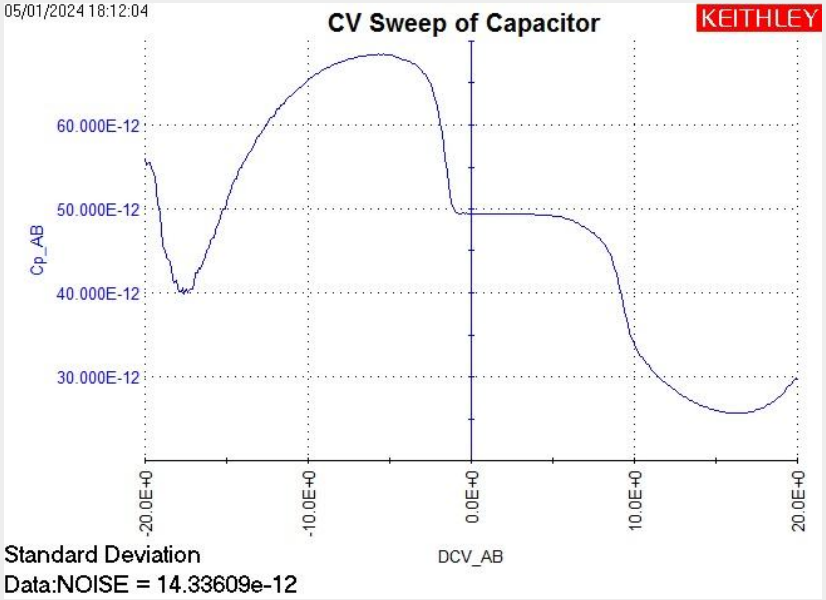
Post Cooling



Initial Chip 417 CV Curve...?

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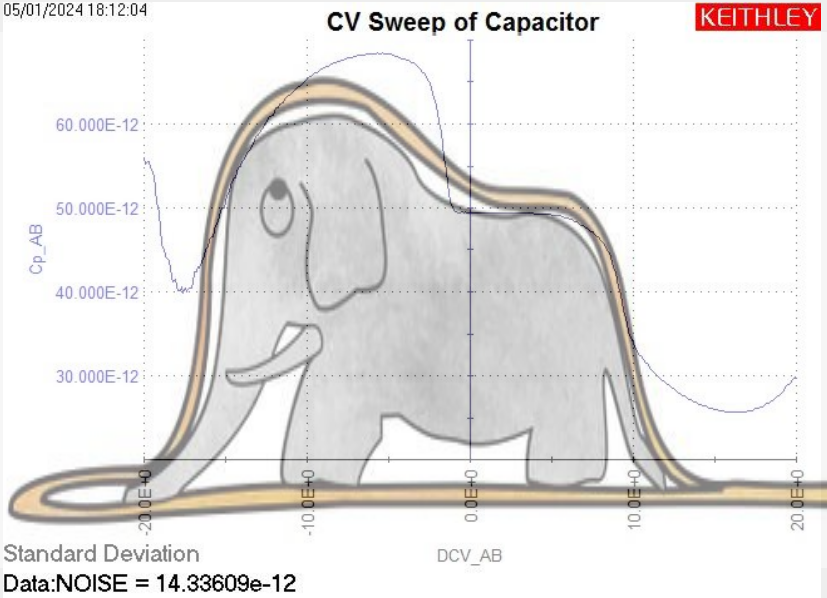
Post Cooling



Initial Chip 417 CV Curve...?

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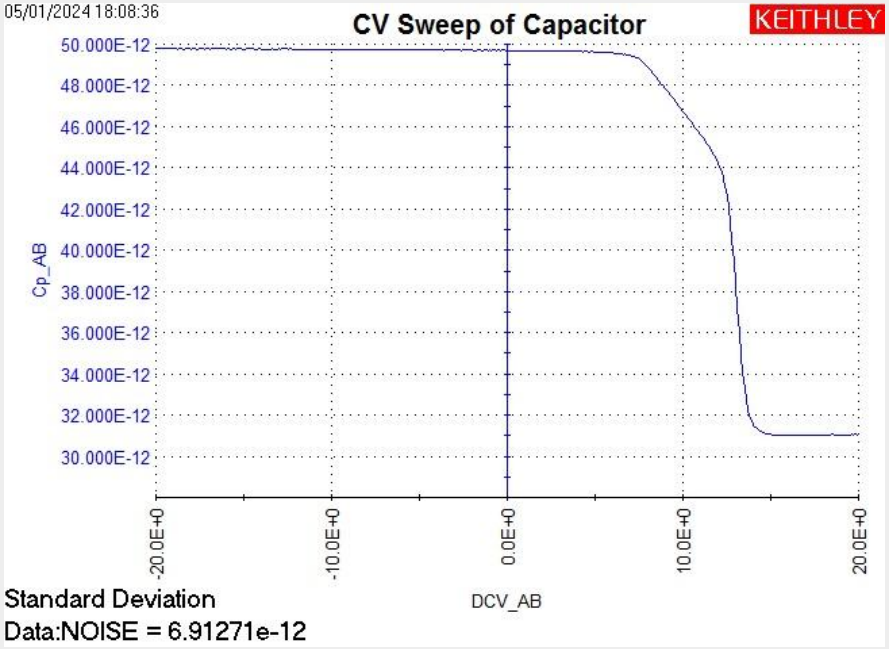
Post Cooling



Second Chip 417 CV Curve with Vth <15V

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Overall results

- CV Curve translated ~5V
  - Although expected a more major translation towards 0V
- Contamination test demonstrates significant ion contamination
  - ∴ our current thermal oxidation method is too “dirty”
- RCA batch included unreliable CV curves
  - Likely stems from CV probing or process variation rather than RCA methods
  - HCl caused heavy leakage
  - RCA also used heavy amounts of solutes and time to prepare
- With all this mind, thermal oxidation in its current state is an undesirable method for oxide growth