Alec Bender

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Education

Carnegie Mellon University Pittsburgh, PA
Master of Science, Electrical and Computer Engineering Dec 2025
Cumulative GPA: 4.00/4.00, Concentration in Integrated Systems

Carnegie Mellon University Pittsburgh, PA
Bachelor of Science, Electrical and Computer Engineering May 2025
Bachelor of Science, Materials Science and Engineering, Minor in Electrical Materials
Cumulative GPA: 3.50/4.00, University Honors

Relevant Coursework: 18-525 Adv. Digital IC Design, 18-726 IC Projects - First Silicon, 18-422 Digital IC Design, 18-740 Modern Computer Architecture, 27-533 Growth & Processing of Semiconductors

Technical Skills

Hardware Design Tools: Cadence Virtuoso/Genus/Innovus, Synopsys VCS/EDA, Calibre, FPGA
Programming Languages: SystemVerilog, Python, C/C++, Tcl, Assembly (x86/ARM/RISC-V), Go, Matlab
Software & Data Science Tools: Linux, Jenkins, JFrog Artifactory, JSON, Pandas, NumPy, CUDA

Experience

IBM | CPU Physical Design and Integration Intern | Austin, TX May 2025 – Present
- Optimized floorplan, placement, and timing for the z18 L3 cache using IBM's internal physical design flow
- Closed the majority of critical timing violations across L3 partitions, reducing worst slack by 86%
- Executed the first full block integration of the L3 cache through collaboration with timing and logic teams

IBM | CPU Clock Physical Design and DevOps Intern | Austin, TX May 2024 – Aug 2024
- Curated and analyzed 12 new clock tree topologies in Cadence Virtuoso for application in IBM microprocessors
- Reduced P11 microprocessor clock power by 4% through FO2 buffer prioritization and identifying fan out power trends
- Automated continuous integration metric aggregation to streamline Release Delivery Automation reports

Argonne National Laboratory | Nanoscale Heterostructures Researcher | Lemont, IL Jun 2022 – Jun 2024
- Generated and trained a CNN image classification pipeline for automated identification of skyrmions in LTEM images
- Attained 95% segmentation accuracy and published results in AIP Advances (2024) – https://doi.org/10.1063/5.0197138

Projects

Tapeout for ASIC Modulation Recognition | 18-525 Adv. Digital IC Design Jan 2025 – May 2025
- Taped-out 1x1mm ASIC modulation recognition system in 28nm TSMC utilizing a Risdual Neural Network (ResNet)
- Developed a 2x1.5mm tapeout-ready ASIC combining the ResNet and Strip Spectral Correlation Algorithm (SSCA)
- Integrated and verified RISC-V CPU, Wishbone bus, SPI, MMIO, ResNet, SSCA, and 250KB Memory
- Improved throughput by 73.3x on 1x1mm ASIC compared to reference FPGA implementation

Tapeout of ASIC Pixel Simulator | 18-620 Design of IoT Systems Aug 2024 – Dec 2024
- Taped-out ASIC pixel sim in 65nm TSMC composed of a DAC, ADC, counter, bias network, and scan chains
- Learned analog mixed signal (AMS) integration Cadence tool flow and completed full chip post-sim verification

RISC-V Pipeline | 18-447 Intro to Computer Architecture Jan 2024 – May 2024
- Built a 13-stage RISC-V R321 ISA pipeline employing caches, forwarding, stalling, and a BTB table
- Tailored pipeline for high frequency computation by optimizing data forwarding during instruction decode

Gate Stack Development Project Lead | 18-669 Hacker Fab Jan 2024 – May 2024
- Led in-house low-cost DIY methods in developing the gate stack for CMU's open-source semiconductor fab facility
- Replaced pre-deposited SiO_2 and poly layers to allow diffusion of N-well in base silicon layer for PMOS production

SRAM | 18-422 Digital IC Design Nov 2023 – Dec 2023
- Designed a standard T architecture SRAM in 45nm GDPK technology with a total capacity of 256 16b data words
- Achieved an access and cycle time of 26.4 FO4, power dissipation of 1mW of 50/50 R/W, and total area of 9.8M λ^2
- Produced one of only 12 fully functional SRAMs out of 25 student submissions, meeting DRC, LVS, and timing specs